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Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

B.Tech

SEM: III - THEORY EXAMINATION (2024 - 2025)

Subject: Computer Organization & Architecture

Time: 3 Hours Max. Marks: 100

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*

1. This Question paper comprises of three Sections -A, B, & C. It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.

2. Maximum marks for each question are indicated on right -hand side of each question.

3. Illustrate your answers with neat sketches wherever necessary.

4. Assume suitable data if necessary.

5. Preferably, write the answers in sequential order.

6. No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.

SECTION-A 20

1. Attempt all parts:-

1-a. The addressing mode which makes use of in-direction pointers is _____ .(CO1.K2) 1

(a) Indirect addressing mode

(b) Index addressing mode

(c) Relative addressing mode

(d) None of above

1-b. The only language which the computer understands is _____ .(CO1,K2) 1

(a) Assembly Language

(b) Binary Language

(c) BASIC

(d) C Language

1-c. If A and B are the inputs of a half adder, the carry is given by _____(CO2,K2) 1

(a) A AND B

(b) A OR B

(c) A XOR B

(d) A EX-NOR B

1-d. IEEE stands for _____.(CO2,K2) 1

(a) Instantaneous Election Electrical Engineering
(b) Institute of Emerging Electrical Engineers
(c) Institute of Emerging Electronic Engineers
(d) Institute of Electrical and electronics engineers

1-e. _____ is the formula for Hit Ratio.(CO3,K2) 1

(a) Hit/(Hit + Miss)
(b) Miss/(Hit + Miss)
(c) (Hit + Miss)/Miss
(d) (Hit + Miss)/Hit

1-f. The next level of memory hierarchy after the L2 cache is _____.(CO3,K2) 1

(a) Secondary storage
(b) Main memory
(c) Register
(d) TLB

1-g. A _____ command is issued to activate the peripheral and to inform it what to do.(CO4,K2) 1

(a) Control
(b) Status
(c) Data output
(d) Data Input

1-h. Instructions that are read from memory by an IOP are sometimes called _____, to distinguish them from instructions that are read by the CPU.(CO4,K2) 1

(a) Commands
(b) Instructions
(c) Program
(d) Subroutine

1-i. The pipelining process is also called as _____.(CO5,K2) 1

(a) Superscalar operation
(b) Assembly line operation
(c) Von Neumann cycle
(d) None of the mentioned

1-j. In the instruction ADD A, B, the answer gets stored in _____(CO5,K2) 1

(a) B
(b) A
(c) Buffer
(d) C

2. Attempt all parts:-

2.a. Define Relative Addressing modes and Base Register Addressing 2

	Mode.(CO1,K3)	
2.b.	Explain Array Multiplier.(CO2,K2)	2
2.c.	Define Hit, Miss and Hit Ratio.(CO3,K2)	2
2.d.	Write the difference between synchronous and asynchronous serial communication. (CO4,K3)	2
2.e.	Define Interrupts and its type in digital system.(CO5,K2)	2

SECTION-B 30

3. Answer any five of the following:-

3-a.	Explain instruction format. Draw its format with Mode field.(CO1.K2)	6
3-b.	Define direct Addressing modes and indirect Addressing Mode used in Computer Architecture.(CO1,K3)	6
3-c.	Represent (1259.125)10 in IEEE single and double precision format.(CO2,K3)	6
3-d.	Show the flow diagram & multiplication process using Booth's Algorithm for (+4) X (+3). (CO2,K3)	6
3.e.	Explain 2D and 2.5D memory organization.(CO3,K2)	6
3.f.	Explain difference between software and hardware interrupts.(CO4,K2)	6
3.g.	Write short notes on Single-instruction, single-data (SISD) systems.(CO5,K2)	6

SECTION-C 50

4. Answer any one of the following:-

4-a.	Draw the block diagrams for Daisy chaining and Independent Centralized Arbitration schemes.(CO1,K2)	10
4-b.	Explain bus organization for seven CPU registers with the help of block diagram and control word.(CO1,K3)	10

5. Answer any one of the following:-

5-a.	Define Carry Look Ahead Adder. Explain with logic diagram.(CO2,K2)	10
5-b.	Sketch the flow diagram of booth multiplication algorithm and Explain it.(CO2,K2)	10

6. Answer any one of the following:-

6-a.	Write short notes on: i) Hardwired control unit ii) Microprogrammed control unit(CO3,K3)	10
6-b.	Explain three address and zero address instruction with example.(CO3,K3)	10

7. Answer any one of the following:-

7-a.	Differentiate between memory mapped I/O and I/O mapped I/O. Explain with block diagram.(CO4,K3)	10
7-b.	What is DMA Controller? Draw and explain the block diagram of DMA Controller.(CO4,K3)	10

8. Answer any one of the following:-

8-a.	Explain Instruction Pipeline and explain with the help of block diagram.(CO5.K2)	10
8-b.	Differentiate between pipeline and parallel processing? Explain with the help of block diagram.(CO5,K3)	10