Printed Page:-03 Subject Code:- AEC0502

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

B.Tech

SEM: V - THEORY EXAMINATION (2024- 2025)

Subject: CMOS Digital Integrated Circuit

Time: 3 Hours Max. Marks: 100

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*

1. This Question paper comprises of three Sections -A, B, & C. It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.

2. Maximum marks for each question are indicated on right -hand side of each question.

3. Illustrate your answers with neat sketches wherever necessary.

4. Assume suitable data if necessary.

5. Preferably, write the answers in sequential order.

6. No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.

SECTION-A 20

1. Attempt all parts:-

1-a. What type of a MOSFET device is ? (CO1,K1) 1

(a) Current-controlled

(b) Voltage-controlled

(c) Voltage-controlled Current source

(d) Voltage-controlled Voltage source

1-b. _____ is normally referred to as ON switches. (CO1,K1) 1

(a) JFET

(b) UJT

(c) Depletion MOSFET

(d) Enhancement MOSFET

1-c. Pull-up network (PUN) connects output node to _____ . (CO2,K1) 1

(a) VDD

(b) Ground

(c) Input

(d) All of these

1-d. An AND terms are realized by _____ connections of NMOS in PDN.(CO2,K1) 1

(a) Series

(b) Parallel

(c) Cascade
(d) Anti-parallel

1-e. Power dissipation in switch logic is _____.(CO3,K1) 1

(a) Less
(b) More
(c) High
(d) Very Less

1-f. In CMOS transmission gates, the NMOS and PMOS transistors are connected in _____.(CO3,K1) 1

(a) Series
(b) Parallel
(c) Point to point
(d) Random

1-g. Circuit designers need _____ circuits. (CO4,K1) 1

(a) tighter
(b) smaller layout
(c) decreased silicon area
(d) all of the mentioned

1-h. In which design all circuitry and all interconnections are designed? (CO4,K1) 1

(a) full custom design
(b) semi-custom design
(c) gate array design
(d) transistor design

1-i. Which Hardware description language is used for ASICs? (CO5,K1) 1

(a) system Verilog
(b) system c
(c) C++
(d) verilog

1-j. _____ is the fundamental architecture block or element of a target PLD.(CO5,K1) 1

(a) System Partitioning
(b) Pre-layout Simulation
(c) Logic cell
(d) Post-layout Simulation

2. Attempt all parts:-

2.a. Explain inversion mode in MOSFET. (CO1,K1) 2

2.b. Draw the truth table of half-adder. (CO2,K1) 2

2.c. Define Complementary Pass Transistor logic (CPL). (CO3,K1) 2

2.d.	What do you understand by Gate array? (CO4,K1)	2
2.e.	What do you mean by DRC, ERC and LVS in ASIC? (CO5,K2)	2

SECTION-B 30

3. Answer any five of the following:-

3-a.	What are the short channel effects and Narrow channel effects? Discuss them in brief.(CO1,K1)	6
3-b.	Realize the boolean function Y= (A+B).C using CMOS logic. (CO1,K2)	6
3-c.	Explain demultiplexer and design 1:2 demupltiplexer using CMOS logic circuit (CO2,K2)	6
3-d.	Describe 8 bit flash type ADC. Determine the number of comparators and resistors required in this. (CO2,K2)	6
3.e.	Implement a NAND and NOR logic gates using Pass transistor logic. (CO3,K3)	6
3.f.	Design a stick diagram for CMOS based NAND gate. (CO4,K3)	6
3.g.	Explain Y Chart in VLSI. (CO5,K2).	6

SECTION-C 50

4. Answer any one of the following:-

4-a.	Explain the voltage transfer characteristics curve of CMOS inverter and explain different regions of operation. (CO1,K2)	10
4-b.	Explain the following terms with neat diagram (i) threshold voltage reduction (ii) punchthrough (iii) channel length modulation. (CO1,K1)	10

5. Answer any one of the following:-

5-a.	Explain the weighted resistor type and R-2R type DAC. (CO2,K2)	10
5-b.	Implement NAND gate based JK flip-flop using CMOS and discuss its working. (CO2,K3)	10

6. Answer any one of the following:-

6-a.	Implement the function Y= (A.B).C+ D using (i) Pseudo-NMOS (ii) Domino CMOS logic. (CO3,K3)	10
6-b.	Design the following circuits using transmission gates (i) D flip-flop (ii) Two-input XOR gate. (CO3,K3)	10

7. Answer any one of the following:-

7-a.	Explain in detail the design hierarchy, regularity, modularity and locality in view of VLSI design methodology. (CO4,K1)	10
7-b.	Draw the flow chart of VLSI Design flow and explain the operation of each step in detail. (CO4,K1)	10

8. Answer any one of the following:-

8-a.	Explain in brief the libraries, floorplanning, placement, routing and verification in ASIC design. (CO5,K1)	10
8-b.	What are the components of a standard cell library? Discuss in detail each of them separately. (CO5,K1)	10