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Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute)

Affiliated to Dr. A.P.J. Abdul Kalam Technical University, Uttar Pradesh, Lucknow

MCA

SEM: I - THEORY EXAMINATION (2021 - 2022)

Subject: Computer System Organization

Time: 03:00 Hours Max. Marks: 100

General Instructions:

1. All questions are compulsory. It comprises three Sections A, B and C.

- Section A - Question No- 1 is objective type question carrying 1 mark each & Question No- 2 is very short type questions carrying 2 marks each.
- Section B - Question No- 3 is Long answer type - I questions carrying 6 marks each.
- Section C - Question No- 4 to 8 are Long answer type - II questions carrying 10 marks each.
- No sheet should be left blank. Any written material after a Blank sheet will not be evaluated/checked.

SECTION A 20

1. Attempt all parts:-

1-a. Which of the following logic operations produce a 0 if the inputs are 1,1 and 0? (CO1) 1

1. OR
2. AND
3. Exclusive OR
4. Exclusive NOR

1-b. The Boolean expression X + X' Y equals (CO1) 1

1. X + Y
2. X + XY
3. Y + YX
4. X' Y + Y' X

1-c. We can construct the common bus system by using (CO2) 1

1. Multiplexers
2. Decoders
3. Encoders
4. Adders

1-d. How many logic operations can be performed by using two variables? (CO2) 1

1. 4
2. 16
3. 32
4. 2

1-e. A microprogrammed control unit (CO3) 1

1. Is faster than a hardwired control unit
2. Facilitates easy implementation of new instructions
3. Is useful when very small programs are to be run
4. Usually refers to the control unit of a microprocessor

1-f. The expression (3 * 4) + (5 * 6) in reverse polish notation is expressed as (CO3) 1

1. 34*56*+

2. 34**+56
3. *34+*56
4. +**3456

1-g. FFFF will be the last memory location in a memory of size (CO4) 1

1. 1K
2. 16K
3. 32K
4. 64K

1-h. The cost of storing a bit is minimum in (CO4) 1

1. Cache
2. Register
3. RAM
4. Magnetic disc

1-i. Which of the following is not a mode of data transfer? (CO5) 1

1. Programmed I/O
2. Interrupt-initiated I/O
3. Direct memory access
4. Hardware-initiated I/O

1-j. A processor that communicates with remote terminals over telephone and other communication media in a serial fashion is called (CO5) 1

1. Input output processor
2. Data communication processor
3. Central processor
4. DMA controller

2. Attempt all parts:-

2.a. Explain Excess-3 and Excess-127 code. (CO1) 2

2.b. Define microoperations. (CO2) 2

2.c. Define the purpose of Program counter. (CO3) 2

2.d. What is register? (CO4) 2

2.e. What is bus arbitration? (CO5) 2

SECTION B 30

3. Answer any five of the following:-

3-a. Determine by means of a truth table the validity of Demorgan's theorem for three variables: (ABC)' = A' +B' +C' (CO1) 6

3-b. List the truth table of a three variable exclusive-OR (odd) function: x= A XOR B XOR C. (CO1) 6

3 Starting from an initial value of R= 11011101, determine the sequence of binary values in R after a logical shift left, followed by a circular shift right, followed by a logical shift right and a circular shift left. (CO2) 6

3 How to design the 4-bit binary incrementer explain using suitable diagram? (CO2) 6

3.e. Explain about register stack organization using suitable diagram and write the microoperations for push and pop operations. (CO3) 6

3.f. What is associate memory? (CO4) 6

3.g. Explain with the block diagram the DMA transfer in a computer system. (CO5) 6

SECTION C 50

4. Answer any one of the following:-

4-a.	Explain multiple bus organization in detail. (CO1)	10
4-b.	Show the step by step multiplication process using Booth algorithm; (-13) X (+15) (CO1)	10
5. Answer any one of the following:-		
5-a.	A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers? (CO2) A. How many multiplexers are there in the bus. B. What size of multiplexers are needed, also tell about selection line	10
5-b.	Design a full adder by using two half adders and explain its functionality. (CO2)	10
6. Answer any one of the following:-		
6	Explain General Register Organization of CPU in detail using suitable diagrams. (CO3)	10
6	An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is; (CO3) a. Direct b. immediate c. relative d. Register indirect e. Index with R1 as index register	10
7. Answer any one of the following:-		
7-a.	Discuss the different mapping techniques used in cache memories and their relative merits and demerits. (CO4)	10
7-b.	What is Memory hierarchy? Explain the purpose to construct such memory hierarchy in digital computers. (CO4)	10
8. Answer any one of the following:-		
8	Explain multithreading. Explain the concept of hardware multithreading and also tell how it is useful with respect to program execution. (CO5)	10
8	Explain Daisy chaining priority. What is the role of Priority in and Priority out signal in daisy chaining? (CO5)	10