Printed Page:-04 **Subject Code:- AEC0404**

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

B.Tech

SEM: IV - THEORY EXAMINATION (2023 - 2024)

Subject: Microprocessor and Microcontroller

Time: 3 Hours **Max. Marks: 100**

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*

1. *This Question paper comprises of* **three Sections -A, B, & C.** *It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.*

2. *Maximum marks for each question are indicated on right -hand side of each question.*

3. *Illustrate your answers with neat sketches wherever necessary.*

4. *Assume suitable data if necessary.*

5. *Preferably, write the answers in sequential order.*

6. *No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.*

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SECTION A **20**

1. Attempt all parts:-

1-a. The circuit used to store one bit of data is known as ___.(CO1) 1

(a) Register

(b) Flip Flop

(c) Counter

(d) None

1-b. How many data lines and address lines are available in 8085? (CO1) 1

(a) 4,8

(b) 8,16

(c) 8,8

(d) 16,32

1-c. What is the function of STC instruction? (CO2) 1

(a) Store to C Register, the value of Accumulator

(b) Set Carry to 1

(c) Clear the Stack pointer

(d) None

1-d. There are _____ general purpose registers in 8085 processor. (CO2) 1

(a) 6

(b) 7

(c) 8

(d) 9

1-e. The internal RAM memory of the 8051 microcontroller is_____. (CO3) 1

(a) 32 bytes

(b) 64 bytes

(c) 128 bytes

(d) 256 bytes

1-f. If we push data onto the stack then the stack pointer _____. (CO3) 1

(a) increases with every push

(b) decreases with every push

(c) Don't get effected

(d) None of these

1-g. Cortex-M3 processor consist of _____ pipeline. (CO4) 1

(a) two stages

(b) three stages

(c) Four stages

(d) five stages

1-h. When the processor is executing in jazelle state, then all instructions are _____bit wide. (CO4) 1

(a) 8

(b) 16

(c) 32

(d) 64

1-i. What is the full form of DSB? (CO5) 1

(a) Data Start Barrier

(b) Data Set Barrier

(c) Data Synchronization Barrier

(d) None of these

1-j. Which one of the following instruction is used as sleep mode feature related 1

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instruction? (CO5)

(a) CMN

(b) WFE

(c) REV

(d) None

2. Attempt all parts:-

2.a.	What is a register? (CO1)	2
2.b.	Name 5 different addressing modes? (CO2)	2
2.c.	Write a short note on timer mode 1 operation of 8051. (CO3)	2
2.d.	Discuss the five features of ARM Cortex M0 processor. (CO4)	2
2.e.	Discuss any two logical instructions of Cortex-M0 processor. (CO5)	2

SECTION B **30**

3. Answer any <u>five</u> of the following:-

3-a.	What do you mean by Harvard and Von Neumann architecture? (CO1)	6
3-b.	Write short note on: a. Virtual Memory b. Magnetic Tape c. Cache Memory. (CO1)	6
3-c.	List the major features of 8085 microprocessor. (CO2)	6
3-d.	What is bus? Explain different types of buses. (CO2)	6
3.e.	What is conditional jump instruction of 8051? Explain various conditions. (CO3)	6
3.f.	Explain the architecture of ARM Cortex M0 microprocessor with a neat diagram. (CO4)	6
3.g.	Explain the classification of instruction set available in ARM processor with example. (CO5)	6

SECTION C **50**

4. Answer any <u>one</u> of the following:-

4-a.	Explain the difference between each of the following: (CO1) i. RAM and ROM ii. RISC and CISC	10
4-b.	Describe the concept of memory hierarchy based on size, cost and speed. (CO1)	10

5. Answer any <u>one</u> of the following:-

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5-a.	Explain the 8085 microprocessor interrupt system in detail. (CO2)	10
5-b.	What is stack and stack pointer? Explain PUSH and POP instructions. (CO2)	10

6. Answer any <u>one</u> of the following:-

6-a.	Explain in detail pin diagram of 8051 microcontroller. (CO3)	10
6-b.	Discuss about the organization of internal RAM and special function registers of 8051 microcontroller in detail. (CO3)	10

7. Answer any <u>one</u> of the following:-

7-a.	How three stage pipeline can be implemented and work efficiently in Cortex M0 processor? (CO4)	10
7-b.	How power efficient and high performance processors can be achieved in ARM Cortex-M0 processor? (CO4)	10

8. Answer any <u>one</u> of the following:-

8-a.	Explain arithmetic and rotate instructions available in ARM Cortex-M0 instruction set. (CO5)	10
8-b.	Mention the instructions used for shift operations. Explain the same using suitable examples. (CO5)	10

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