Printed Page:- 04 **Subject Code:- AEC0301**

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

B.Tech

SEM: III - CARRY OVER THEORY EXAMINATION - AUGUST 2023

Subject: Digital System Design

Time: 3 Hours **Max. Marks: 100**

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*

1. *This Question paper comprises of* **three Sections -A, B, & C.** *It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.*

2. *Maximum marks for each question are indicated on right -hand side of each question.*

3. *Illustrate your answers with neat sketches wherever necessary.*

4. *Assume suitable data if necessary.*

5. *Preferably, write the answers in sequential order.*

6. *No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.*

SECTION A **20**

1. Attempt all parts:-

1-a. A switching function f(A, B, C, D) = A'B'CD + A'BC'D + AB'C'D + AB'CD + A'BCD can also be written as (CO1) 1

(a) Σm(1, 3, 5, 7, 9)

(b) Σm(3, 5, 7, 9, 11)

(c) Σm(3, 5, 9, 11, 13)

(d) None of these

1-b. The gray code is a _____ (CO1) 1

(a) weighted code

(b) reflexsive code

(c) self complementing code

(d) unit distance code

1-c. Which One is not the outcome of magnitude comparator (CO2) 1

(a) a > b

(b) a – b

(c) a < b

(d) a = b

1-d. Number of input and output in Full Subtractor are .....respectively. (CO2) 1

(a) 2 and 2

(b) 2 and 3

(c) 3 and 2

(d) 3 and 3

1-e. The first step of the analysis procedure of SR latch is to _____ (CO3) 1

(a) label inputs

(b) label outputs

(c) label states

(d) label tables

1-f. The output response of the sequential circuit depends upon _____ (CO3) 1

(a) Only Present input

(b) Past input

(c) Present input and passed output

(d) None of the above

1-g. Which of the following is the most widely employed logic family? (CO4) 1

(a) Emitter-coupled logic

(b) Transistor-transistor logic

(c) PMOS logic

(d) NMOS logic

1-h. Number of output configuration in TTL Nand Gate is------. (CO4) 1

(a) 3

(b) 2

(c) 1

(d) 4

1-i. Which memory is necessary to refresh many times in one second? (CO5) 1

(a) Dynamic RAM

(b) Static RAM

(c) EPROM

(d) ROM

1-j. Which device is not used as PLD ? (CO5) 1

(a) PROM

(b) PLA

(c) SRAM

(d) PAL

2. Attempt all parts:-

2.a.	Write the Demorgan's Theoram. (CO1)	2
2.b.	Design 8:1 Mux using two 4:1 Mux. (CO2)	2
2.c.	Write the advantages of sequential circuits? (CO3)	2
2.d.	Define Fan-in and Fan-out of logic family. (CO4)	2
2.e.	Compare EPROM to EEPROM. (CO5)	2

SECTION B **30**

3. Answer any <u>five</u> of the following:-

3-a.	Develop the logic diagram using NAND gate of the Boolean expression Y = AC' +A B'+BC (CO1)	6
3-b.	Perform the Hexadecimal addition and subtraction of 2BD.1 H and 3EF.9 H. (CO1)	6
3-c.	Explain half subtractor with proper logic circuit diagram. (CO2)	6
3-d.	Implement Full adder using Two half adders. (CO2	6
3.e.	Draw the truth table of all 4 types of flip-flop. (CO3)	6
3.f.	Explain the Totem pole output of TTL logic family. (CO4)	6
3.g.	Design a 4-bit binary to gray code converter using PROM. (CO5)	6

SECTION C **50**

4. Answer any <u>one</u> of the following:-

4-a.	Represent the decimal number $(396)_{10}$ in (CO1) (i) Binary code (straight binary) (ii) BCD code (iii) Excess-3 code (iv) Octal code (v) Hexa decimal code	10
4-b.	Realize the all basic gates using only NAND gates. (CO1)	10

5. Answer any <u>one</u> of the following:-

5-a.	Design and implement a 2-bit magnitude comparator. (CO2)	10
5-b.	Design 3:8 line Decoder using logic gates. (CO2)	10

6. Answer any <u>one</u> of the following:-

6-a.	Convert J-K flip-flop into D flip-flop. (CO3)	10
6-b.	Explain ring counter in detail.(CO3)	10

7. Answer any <u>one</u> of the following:-

7-a.	Draw the basic gate of ECL logic family and explain its advantages and disadvantages. (CO4)	10
7-b.	Compare TTL, ECL and CMOS logic families. (CO4)	10

8. Answer any <u>one</u> of the following:-

8-a.	Draw the block diagram PLA and explain the function of each blocks. (CO5)	10
8-b.	Compare PROM, PAL and PLA in details. (CO5)	10