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Subject Code:- AMTVL0211

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

M.Tech.

SEM: II - THEORY EXAMINATION (2021 - 2022)

Subject: VLSI Testing and Testability

Time: 3 Hours | Max. Marks: 70

General Instructions:

1. The question paper comprises three sections, A, B, and C. You are expected to answer them as directed.
2. Section A - Question No- 1 is 1 marker & Question No- 2 carries 2 marks each.
3. Section B - Question No-3 is based on external choice carrying 4 marks each.
4. Section C - Questions No. 4-8 are within unit choice questions carrying 7 marks each.
5. No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.

SECTION A 15

1. Attempt all parts:-

1-a. The fraction or percentage of some good chips which are rejected is called ______. (CO1) 1

(a) Reject Rate

(b) Rejection Ratio

(c) Yield loss

(d) None of these

1-b. Automatic test pattern generators depend on___________. (CO2) 1

(a) map design

(b) layout design

(c) logic domain

(d) testing domain

1-c. The full form of LSSD. (CO3) 1

(a) Level scan sub design

(b) Level sensitive scan design

(c) Level sensitive sub design

(d) none of these

1-d. If a path exists between two multiple logic blocks that are never selected at the same time then the path is considered as___________. (CO4) 1

(a) Critical Path

(b) False Path

(c) Multicycle Path

(d) none of these

1-e. Initialization of the test pattern generator to all 1's generate ___________. (CO5) 1

(a) global reset

(b) clear

(c) toggle

(d) buffer

2. Attempt all parts:-

2.a.	Write the different challenges in VLSI testing. (CO1)	2
2.b.	Define sensitized line and sensitized path. (CO2)	2
2.c.	What are the scan based test techniques? (CO3)	2
2.d.	What is the importance of memory testing? (CO4)	2
2.e.	What are self test techniques? (CO5)	2

SECTION B 20

3. Answer any five of the following:-

3-a.	Differentiate single stuck and multiple stuck at fault models. (CO1)	4
3-b.	With the help of neat sketches of rise and fall time test, set up and hold time test explain AC parametric test. (CO1)	4
3-c.	Write all the steps of a PODEM algorithm. (CO2)	4
3-d.	Draw and explain the flow chart of an ATPG system. (CO2)	4
3.e.	Discuss the various problems associated with sequential circuit testing. (CO3)	4
3.f.	Describe the various types of coupling fault in RAM fault models. (CO4)	4
3.g.	Discuss the differences between exhaustive and pseudo exhaustive test generation methods of BIST. (CO5)	4

SECTION C 35

4. Answer any one of the following:-

4-a. Explain the methods of equivalence fault collapsing and dominant fault collapsing with 7

suitable examples. (CO1)

4-b. Implement a full adder using AND, OR and NOT gates, and determine the total number of single stuck at faults and multiple stuck at faults. (CO1) 7

5. Answer any <u>one</u> of the following:-

5-a. How can you eliminate the hazards in any circuit output? Explain with suitable example. (CO2) 7

5-b. How the path sensitization method is used to generate a test pattern for combinational circuits? (CO2) 7

6. Answer any <u>one</u> of the following:-

6-a. Show the basic cell of a boundary-scan register. Describe different modes of its operation. (CO3) 7

6-b. Discuss the procedure of ATPG and testing using partial scan chain in a sequential circuit. (CO3) 7

7. Answer any <u>one</u> of the following:-

7-a. What is robust test? Explain the condition of robust test with an example. (CO4) 7

7-b. Elaborate a comparative analysis of various types of RAM testing algorithms. (CO4) 7

8. Answer any <u>one</u> of the following:-

8-a. Explain with diagram syndrome checking and signature analysis compression techniques used in a BIST environment. (CO5) 7

8-b. With the help of a neat diagram explain the working of multiple input signature register (MISR). (CO5) 7