Printed Page:- 03 **Subject Code:- AMTVL0215**

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

M.Tech

SEM: II - THEORY EXAMINATION (2022-2023)

Subject: Nanoscale Devices: Modeling & Simulation

Time: 3 Hours **Max. Marks: 70**

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*

1. *This Question paper comprises of* **three Sections -A, B, & C.** *It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.*

2. *Maximum marks for each question are indicated on right -hand side of each question.*

3. *Illustrate your answers with neat sketches wherever necessary.*

4. *Assume suitable data if necessary.*

5. *Preferably, write the answers in sequential order.*

6. *No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.*

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SECTION A **15**

1. Attempt all parts:-

1-a. Short-channel effects can be distinguished. (CO1) 1

(a) drain-induced barrier lowering

(b) surface scattering

(c) velocity saturation

(d) all of above

1-b. Measurement of Hall coefficient enables the determination of (CO2) 1

(a) Mobility of charge carriers

(b) Type of conductivity and concentration of charge carriers

(c) Temperature coefficient and thermal conductivity

(d) None of the above

1-c. The gap between the two walls of a double walled carbon nanotube comprised of (5,5) inner tube and (12,12) outer tube in 'nano meter' is equal to (CO3) 1

(a) 6.78

(b) 4.76

(c) .678

(d) .476

1-d. Technology in which use of a layered silicon-insulator-silicon substrate in place of conventional silicon substrates in semiconductor manufacturing is referred as (CO4) 1

(a) SOI

(b) SOS

(c) IOI

(d) SiO

1-e. .....analog-to-digital converters (ADCs) use no clock signal, because there is no timing of sequencing require (CO5) 1

(a) Flash

(b) Actuator

(c) Bipolar

(d) Dual

2. Attempt all parts:-

2.a. What do you mean by Plasma Oxidation? (CO1) 2

2.b. What is the width of the depletion layer at the onset of inversion? (CO2) 2

2.c. Why nanowires are important in devices? (CO3) 2

2.d. Is FD-SOI compatible with cost-sensitive? (CO4) 2

2.e. What is Logic Gates? (CO5) 2

SECTION B **20**

3. Answer any <u>five</u> of the following:-

3-a. Explain the working principle of Quantum effects with suitable diagram (CO1) 4

3-b. How to overcome the noise problem in MOSFET Scaling? (CO1) 4

3-c. Write the boundary conditions for minimum gate insulator thickness in the DG MOS system (CO2) 4

3-d. Enlist the problem associated with Miller overlap capacitance (CO2) 4

3.e. Explain the band structure of graphene. (CO3) 4

3.f. How we calculate the performance of single gate SOI? (CO4) 4

3.g. What is op-amp and write its applications? (CO5) 4

SECTION C **35**

4. Answer any <u>one</u> of the following:-

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4-a.	Discuss the Narrow channel effect in detail and justify that due to this effect how threshold voltage is greater than normal channel devices? (CO1)	7
4-b.	What do you mean by ITRS? How its report set a benchmark for the semiconductor industry? (CO1)	7

5. Answer any <u>one</u> of the following:-

5-a.	Explain semiconductor thickness effect in detail. Also draw the graph between energy and semiconductor thickness (CO2)	7
5-b.	Explain Two-dimensional confinement in MOS structure with suitable diagram (CO2)	7

6. Answer any <u>one</u> of the following:-

6-a.	Explain Schottky barrier carbon nanotube FETs with suitable diagram (CO3)	7
6-b.	Define I-V characteristics for carbon nanotube FETs. (CO3)	7

7. Answer any <u>one</u> of the following:-

7-a.	Explain advanced multi-gate devices in detail. (CO4)	7
7-b.	Explain the total ionizing dose effects on various gate devices. (CO4)	7

8. Answer any <u>one</u> of the following:-

8-a.	Explain the impact of device performance on digital circuits. (CO5)	7
8-b.	Write the short notes on - (CO5) i) Band gap voltage reference ii) Signal to Noise ratio and its practical significance iii) Flicker Noise calculation process	7

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