Printed Page:- 03 **Subject Code:- AMTCSE0201**

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

M.Tech

SEM: II - THEORY EXAMINATION (2022-2023)

Subject: High Performance Computing

Time: 3 Hours **Max. Marks: 70**

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*

1. *This Question paper comprises of* **three Sections -A, B, & C.** *It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.*

2. *Maximum marks for each question are indicated on right -hand side of each question.*

3. *Illustrate your answers with neat sketches wherever necessary.*

4. *Assume suitable data if necessary.*

5. *Preferably, write the answers in sequential order.*

6. *No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.*

SECTION A **15**

1. Attempt all parts:-

1-a. VLIW processors rely on CO1 1

(a) 1.Compile time analysis

(b) 2.Initial time analysis

(c) 3.Final time analysis

(d) 4.id time analysis

1-b. The n × n matrix is partitioned among n processors, with each processor storing complete ___ _ of the matrix. CO2 1

(a) 1. Row

(b) 2. column

(c) 3. both

(d) 4.depend on processor

1-c. In a broadcast and reduction on a balanced binary tree reduction is done in __ CO3 1

(a) 1. recursive order

(b) 2. straight order

(c) 3. vertical order

(d) 4.parallel order

1-d. which problems can be handled by recursive decomposition CO4 1

(a) 1. backtracking

(b) 2. greedy method

(c) 3. divide and conquer problem

(d) 4.branch and bound

1-e. The style of parallelism supported on GPUs is best described as CO5 1

(a) 1. MISD – Multiple Instruction Single Data

(b) 2. SIMT – Single Instruction Multiple Thread

(c) 3. SISD – Single Instruction Single Data

(d) 4.MIMD

2. Attempt all parts:-

2.a. Elaborate Computing performance? CO1 2

2.b. Define the symmetric multi processor? CO2 2

2.c. Explain Control structure of parallel platform in details? CO3 2

2.d. Define latency and bandwidth of memory? CO4 2

2.e. How to identify the bottle networks CO5 2

SECTION B **20**

3. Answer any <u>five</u> of the following:-

3-a. What is complexity? CO1 4

3-b. What are the limitations of memory system performance? CO1 4

3-c. Define the co-operative threads? CO2 4

3-d. Write and Explain the cache-coherence protocols names? CO2 4

3.e. What are different partitioning techniques used in Matrix-Vector Multiplication CO3 4

3.f. Describe Uniform Memory access and Non uniform memory access? CO4 4

3.g. Define Memory? Explain restructuring of the memory hierarchy. CO5 4

SECTION C **35**

4. Answer any <u>one</u> of the following:-

4-a. What are the classifications of interconnection networks? CO1 7

4-b.	Give the Characteristics of tasks in details? CO1	7

5. Answer any <u>one</u> of the following:-

5-a.	Give the two names architectural classifications of fetching. Elaborate? CO2	7
5-b.	Define the RoadRunner computer. Explain? CO2	7

6. Answer any <u>one</u> of the following:-

6-a.	Explain instruction prefetch. CO3	7
6-b.	Discuss in detail about the various design issues of pipeline processors. CO3	7

7. Answer any <u>one</u> of the following:-

7-a.	Explain multi-core processors. Discuss different types of multi-core processors? CO4	7
7-b.	What are the Synchronization methods? Explain. CO4	7

8. Answer any <u>one</u> of the following:-

8-a.	Explain memory hierarchy. Also how will you apply this memory hierarchy to transaction specific memory design? CO5	7
8-b.	Write down principles of message passing programming. CO5	7