Printed Page:- 03 **Subject Code:- AMTVL0202**

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

M.Tech

SEM: II - THEORY EXAMINATION (2022-2023)

Subject: Low Power VLSI Design

Time: 3 Hours **Max. Marks: 70**

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*

1. *This Question paper comprises of* **three Sections -A, B, & C.** *It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.*

2. *Maximum marks for each question are indicated on right -hand side of each question.*

3. *Illustrate your answers with neat sketches wherever necessary.*

4. *Assume suitable data if necessary.*

5. *Preferably, write the answers in sequential order.*

6. *No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.*

SECTION A **15**

1. Attempt all parts:-

1-a. Under an input ramp signal, a first order analysis of the short-circuit current reveals that the energy dissipated is _____. (CO1) 1

(a) Eshort =β/12 x τ(Vtp –Vtn)3

(b) Eshort =β x τ(Vtp –Vtn)3

(c) Eshort =β/12 (Vtp –Vtn)

(d) None of these

1-b. How many NMOS and PMOS are required for 2-input CMOS NAND gate? (CO2) 1

(a) 4

(b) 2

(c) 8

(d) None of these

1-c. The J-K flip flops has _____ memory. (CO3) 1

(a) Temporary

(b) Random

(c) Non random

(d) True

1-d. MAR stands for _____. (CO4) 1

(a) Memory address register

(b) Main address register

(c) Main accessible register

(d) Memory accessible register

1-e. Consider an ideal MOSFET. If Vgs = 0V, then Id = ? (CO5) 1

(a) Zero

(b) Maximum

(c) Id(on)

(d) Idd

2. Attempt all parts:-

2.a. What is W/ L ratio? (CO1) 2

2.b. How do you find the capacitive power? (CO2) 2

2.c. What is finite state machine? (CO3) 2

2.d. Why is SRAM called static? (CO4) 2

2.e. How the propogation delay get affected by increasing fanout? (CO5) 2

SECTION B **20**

3. Answer any <u>five</u> of the following:-

3-a. Draw the CMOS schematic for the function: Y=(ab+bc+de)'. (CO1) 4

3-b. Write short notes on impact of technology scaling. (CO1) 4

3-c. Write short notes on probabilistic power analysis techniques. (CO2) 4

3-d. What is the first step in a Monte Carlo analysis? (CO2) 4

3.e. Explain the Standard cell design and cell libraries? (CO3) 4

3.f. What do you understand by flow graph transformation? (CO4) 4

3.g. Differentiate between zero skew and tolerable skew. (CO5) 4

SECTION C **35**

4. Answer any <u>one</u> of the following:-

4-a. How is CMOS logic implemented? Explain in details. (CO1) 7

4-b. What is activity factor ?Explain in details. (CO1) 7

5. Answer any <u>one</u> of the following:-

5-a.	What is probabilistic simulation? Explain in detail. (CO2)	7
5-b.	Why leakage power dissipation has become an important issue in deep submicron technology? (CO2)	7

6. Answer any <u>one</u> of the following:-

6-a.	With the help of block diagram explain architecture of bus invert encoding in details. (CO3)	7
6-b.	Draw the state flow or transition diagram for a JK flip-flop and also give the truth table associated with it. (CO3)	7

7. Answer any <u>one</u> of the following:-

7-a.	What is operator reduction? Explain in details. (CO4)	7
7-b.	What is the difference between power consumption and power dissipation? (CO4)	7

8. Answer any <u>one</u> of the following:-

8-a.	Explain power dissipation in clock distribution in detail. (CO5)	7
8-b.	Explain Algorithmic Level analysis and optimization in detail. (CO5)	7