Printed Page:- 03 **Subject Code:- AMTVL0201**

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

M.Tech

SEM: II - THEORY EXAMINATION (2023- 2024)

Subject: Digital Design Using FPGA and CPLD

Time: 3 Hours **Max. Marks: 70**

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*

1. *This Question paper comprises of* **three Sections -A, B, & C.** *It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.*

2. *Maximum marks for each question are indicated on right -hand side of each question.*

3. *Illustrate your answers with neat sketches wherever necessary.*

4. *Assume suitable data if necessary.*

5. *Preferably, write the answers in sequential order.*

6. *No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.*

SECTION A **15**

1. Attempt all parts:-

1-a. What happens when input is high in FSM? (CO1) 1

(a) Change of state

(b) No transition in state

(c) Remains in a single state

(d) Invalid state

1-b. Memory element of asynchronous circuits are_____. (CO2) 1

(a) Clocked Flip-Flops

(b) Latches

(c) Clock Pulses

(d) Un-clocked Flip-Flops

1-c. A flip flop store _____bits of information. (CO3) 1

(a) 1

(b) 2

(c) 3

(d) 4

1-d. In FPGA, vertical and horizontal directions are separated by _____. (CO4) 1

(a) line

(b) Channel

(c) Strobe

(d) Flip-Flop

1-e. Once a PAL has been programmed: (CO5) 1

(a) its outputs are only active HIGHs

(b) it cannot be programmed

(c) its outputs are only active LOWs

(d) its logic capacity is lost

2. Attempt all parts:-

2.a. What do you mean by state table or the state diagram? (CO1) 2

2.b. What is the difference between synchronous and asynchronous circuit? (CO2) 2

2.c. What do you understand by the term flash memory?(CO3) 2

2.d. Write two advantages of FPGA? (CO4) 2

2.e. What do you mean by Logic Expander? (CO5) 2

SECTION B **20**

3. Answer any <u>five</u> of the following:-

3-a. Describe Moore Model for FSM design with the help of an example.(CO1) 4

3-b. Describe Mealy Model for FSM design with the help of an example. (CO1) 4

3-c. How the race around condition in a JK flip-flop can be eliminated? (CO2) 4

3-d. Discuss about static and dynamic hazards in asynchronous sequential circuits.(CO2) 4

3.e. Write short notes on CPLD programming. (CO3) 4

3.f. Draw architecture of XILINX XC4000 and discuss it.(CO4) 4

3.g. Discuss Cypress FLASH 370 Macro-cell in brief.(CO5) 4

SECTION C **35**

4. Answer any <u>one</u> of the following:-

4-a. Draw Mealy state machine for 3 bit Down Counter and the corresponding state table. (CO1) 7

4-b. What do you mean by state assignment? Explain its types with the help of 7

examples.(CO1)

5. Answer any <u>one</u> of the following:-

5-a.	What are the drawbacks of asynchronous sequential circuit? Give the design procedure for asynchronous sequential circuit and illustrate it's applications.(CO2)	7
5-b.	Design a synchronous counter that counts the sequence 000,001,010,011,100,101,110,111,000 Using T flip-flop.(CO2)	7

6. Answer any <u>one</u> of the following:-

6-a.	Classify Memories and explain EPROM in detail. (CO3)	7
6-b.	What do you understand by the ROM? Discuss in detail about NAND based ROM.(CO3)	7

7. Answer any <u>one</u> of the following:-

7-a.	Write some difference between Custom Chips, Standard Cells, and Gate Arrays with diagram. (CO4)	7
7-b.	Design Full Subtractor using Xilinx XC 4000.(CO4)	7

8. Answer any <u>one</u> of the following:-

8-a.	Describe in detail ALTERA FLEX 10K Logic Array Block. (CO5)	7
8-b.	Design & Implement the Boolean Expression Y=AB+BC+CA on CPLD. (CO5)	7