Printed Page:- 03 **Subject Code:- AMTVL0215**

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

M.Tech

SEM: II - THEORY EXAMINATION (2023 - 2024)

Subject: Nanoscale Devices: Modeling & Simulation

Time: 3 Hours **Max. Marks: 70**

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*

1. *This Question paper comprises of* **three Sections -A, B, & C.** *It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.*

2. *Maximum marks for each question are indicated on right -hand side of each question.*

3. *Illustrate your answers with neat sketches wherever necessary.*

4. *Assume suitable data if necessary.*

5. *Preferably, write the answers in sequential order.*

6. *No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.*

SECTION A **15**

1. Attempt all parts:-

1-a. If the depletion-layer widths (xdS, xdD) of the source and drain junction and L is Channel length then In DIBL case (CO1) 1

(a) xdS + xdD = L

(b) xdS + xdD > L

(c) xdS + xdD < L

(d) xdS - xdD < L

1-b. In MOS lateral Electric field generated due to_____ (CO2) 1

(a) Gate voltage

(b) drain to sourese voltage

(c) barrier potential

(d) None of these

1-c. In Twin Silicon Nanowire FET, gate stack is of number ____ (CO3) 1

(a) 1

(b) 2

(c) 3

(d) 4

1-d. Stray capacitance is also named as_____ (CO4) 1

(a) fixed capacitance

(b) parasitic capacitance

(c) electrolyte capacitance

(d) variable capacitance

1-e. A transconductance amplifier is also called _____. (CO5) 1

(a) current to voltage convertor

(b) voltage to current convertor

(c) resistor

(d) inductor

2. Attempt all parts:-

2.a. Discuss the problem associated with high-K materials. (CO1) 2

2.b. Enlist the significance of Semiconductor thickness effect. (CO2) 2

2.c. Why nanowires are important in devices? (CO3) 2

2.d. How does SOI technology improve the performance of a circuit? (CO4) 2

2.e. Define CMRR? and enlist its significance. (CO5) 2

SECTION B **20**

3. Answer any <u>five</u> of the following:-

3-a. What are the differences between FDSOI and PDSOI? (CO1) 4

3-b. Write a short note on quantum effect and volume inversion. (CO1) 4

3-c. Write the Modeling assumptions for double gate MOS system. (CO2) 4

3-d. How one-dimensional electron gas formed? (CO2) 4

3.e. What are the characteristics of Si nanowires? (CO3) 4

3.f. Drive the expression for Drain current of CMOS with suitable diagram. (CO4) 4

3.g. Explain in brief the principle of operation of successive Approximation ADC. (CO5) 4

SECTION C **35**

4. Answer any <u>one</u> of the following:-

4-a. What do you mean by drain punch through condition? Explain it with suitable diagram.(CO1) 7

4-b.	What is the significance of interconnects in MOS devices and also enlist its types.(CO1)	7

5. Answer any <u>one</u> of the following:-

5-a.	What is corner effect? Write the condition when it vanished out. (CO2)	7
5-b.	How FinFET differ from MIGFET? Enlist the advantage and disadvantage of FinFET. (CO2)	7

6. Answer any <u>one</u> of the following:-

6-a.	Explain the applications of nanowires in biomedical and electronic devices. (CO3)	7
6-b.	What is Schottky barrier? Discuss the carbon nano tube FETs and draw the output characteristics. (CO3)	7

7. Answer any <u>one</u> of the following:-

7-a.	Explain transient effects in SOI devices. (CO4)	7
7-b.	How total ionizing dose effects work in Dual-gate SOI? Explain in detail with suitable diagram? (CO4)	7

8. Answer any <u>one</u> of the following:-

8-a.	What is the importance of Slew Rate for operational Amplifier? Enlist other parameter for operational Amplifier and its practical significance. (CO5)	7
8-b.	Discuss the operation of VCO and LNA and also write the designing step for LNA.(CO5)	7