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NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute)

Affiliated to Dr. A.P.J. Abdul Kalam Technical University, Uttar Pradesh, Lucknow

M.TECH

FIRST YEAR (SEMESTER-II) THEORY EXAMINATION (2020-2021)

(Objective Type)

Subject Code: AMTVL0211 **Max. Mks. : 40**

Subject: VLSI Testing and Testability **Time : 70 Minutes**

General Instructions:

All questions are compulsory.

Question No- 1 to 5 are objective type question carrying 2 marks each.

Question No- 6 to 20 are also objective type/Glossary based question carrying 2 marks each.

Q.No	Question Content	Question Image	Category	Sub Category	Marks	Type	Difficulty	Correct	Option1	Option2	Option3	Option4
1	Parametric testing is concerned with the parameters of the circuit such as _____		Single Choice Questions	Single Choice Questions	2	Single Choice	Smart	current and voltage	Resistance	Capacitance	current and voltage	None of these
2	D algorithm is based on		Single Choice Questions	Single Choice Questions	2	Single Choice	Smart	existence of one fault and one good machine	existence of one fault machine	existence of one fault and one good machine	existence of one good machine	existence of two fault machine alone
3	The boundary scan path is provided with		Single Choice Questions	Single Choice Questions	2	Single Choice	Smart	serial input pads	serial input pads	parallel input pads	parallel output pads	buffer pads
4	IDDQ Testing detects faults by monitoring		Single Choice Questions	Single Choice Questions	2	Single Choice	Smart	Quiscent current	Leakage current	Voltage	Quiscent current	None of these
5	Built-in self test aims to		Single Choice Questions	Single Choice Questions	2	Single Choice	Smart	all of these	reduce test pattern generation cost	reduce volume of test data	reduce test time	all of these
6	If all tests of some fault F1 detect another fault F2, then F2 is said to ………… F1.		Glossary I	Glossary I	2	Single Choice	Brilliant	Dominate	Fault simulator	Fault coverage	Dominate	
7	…………….....is an essential tool for test development.		Glossary I	Glossary I	2	Single Choice	Brilliant	Fault simulator	Fault simulator	Fault coverage	Dominate	
8	………………. is the fraction (or percentage) of modeled faults detected by test vectors.		Glossary I	Glossary I	2	Single Choice	Brilliant	Fault coverage	Fault simulator	Fault coverage	Dominate	
9	PODEM express the search space in terms of assignment to the …………….. only.		Glossary II	Glossary II	2	Single Choice	Brilliant	primary inputs	exponentially	primary inputs	error	
10	D – algorithm is …………….. complex to the number of internal circuit nodes.		Glossary II	Glossary II	2	Single Choice	Brilliant	exponentially	exponentially	primary inputs	error	
11	A defect is an …….. introduced into a device during the manufacturing process.		Glossary II	Glossary II	2	Single Choice	Brilliant	error	exponentially	primary inputs	error	
12	Ad-hoc design method is not suitable for ……… circuits.		Glossary III	Glossary III	2	Single Choice	Brilliant	large	subset	large	ATPG	
13	The process of generating a test pattern for a specific fault using some type of algorithm is known as ……………..		Glossary III	Glossary III	2	Single Choice	Brilliant	ATPG	subset	large	ATPG	
14	In partial scan approach only a ……….. of flip-flops is scanned.		Glossary III	Glossary III	2	Single Choice	Brilliant	subset	subset	large	ATPG	
15	A test algorithm is a ……………. of test elements.		Glossary IV	Glossary IV	2	Single Choice	Brilliant	finite sequence	path delay fault	current	finite sequence	

Q.No	Question Content	Question Image	Category	Sub Category	Marks	Type	Difficulty	Correct	Option1	Option2	Option3	Option4
16	A path whose propagation delay exceeds the specified worst case delay is said to have ………………..		Glossary IV	Glossary IV	2	Single Choice	Brilliant	path delay fault	path delay fault	current	finite sequence	
17	IDDQ testing detects the leak by picking up on any increased magnitude of the …….. , which is easily shown due to semiconductor manufacturing faults.		Glossary IV	Glossary IV	2	Single Choice	Brilliant	current	path delay fault	current	finite sequence	
18	……….. is an additional active area due to test controller, pattern generator, response evaluator and testing of BIST hardware.		Glossary V	Glossary V	2	Single Choice	Brilliant	area overhead	BIST	compression	area overhead	
19	The main pattern generation techniques of …….. are Stored Patterns, Exhaustive Patterns, Pseudo exhaustive Pattern, Pseudo random Pattern.		Glossary V	Glossary V	2	Single Choice	Brilliant	BIST	BIST	compression	area overhead	
20	………. is a reversible process used to reduce the size of the response.		Glossary V	Glossary V	2	Single Choice	Brilliant	compression	BIST	compression	area overhead	