Printed Page:-03 Subject Code:- BMCA0201

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

MCA

SEM: II - THEORY EXAMINATION (2024 - 2025)

Subject: Computer System & Organization

Time: 3 Hours Max. Marks: 100

General Instructions:

IMP: Verify that you have received the question paper with the correct course, code, branch etc.

1. This Question paper comprises of three Sections -A, B, & C. It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.
2. Maximum marks for each question are indicated on right -hand side of each question.
3. Illustrate your answers with neat sketches wherever necessary.
4. Assume suitable data if necessary.
5. Preferably, write the answers in sequential order.
6. No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.

SECTION-A 20

1. Attempt all parts:-

1-a. The radix of a Octal number is: (CO1, K1) 1

(a) 2
(b) 10
(c) 8
(d) 16

1-b. A+B=B+A is a - (CO1, K2) 1

(a) Associative law
(b) Commutative law
(c) Idempotent law
(d) None

1-c. The half adder is a type of _____ (CO2, K2) 1

(a) Combinational circuit
(b) Sequential circuit
(c) CPU
(d) None

1-d. Which among the following is an arithmetic microoperation. (CO2, K2) 1

(a) R1<-R2+1
(b) R1<-R2-1
(c) R1<-R2'+1

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(d) All of the above

1-e. The functions of execution and sequencing are performed by using- (CO3, K2) 1

(a) Input Signal
(b) Output Signal
(c) Control Signal
(d) All of the above

1-f. CISC stands for- (CO3, K1) 1

(a) Complex Information Sensed CPU
(b) Complex Instruction Set Computer
(c) Complex Intelligence Sensed CPU
(d) Complex Instruction Set CPU

1-g. ROM is a: (CO4, K1) 1

(a) Temporary storage
(b) Volatile storage
(c) Non volatile and permanent storage
(d) Volatile and permanent storage

1-h. Cache performance is measured in terms of - (CO4, K1) 1

(a) Throughput
(b) Thrash
(c) Hit Ratio
(d) Miss Ratio

1-i. The method which offers higher speeds of I/O transfers is _____ (CO5, K2) 1

(a) Interrupts
(b) Memory mapping
(c) Program-controlled I/O
(d) DMA

1-j. In memory-mapped I/O _____ (CO5, K1) 1

(a) The I/O devices have a separate address space
(b) The I/O devices and the memory share the same address space
(c) A part of the memory is specifically set aside for the I/O operation
(d) The memory and I/O devices have an associated address space

2. Attempt all parts:-

2.a. Specify the purpose of Buffer logic gate. (CO1, K2) 2

2.b. Define Address bus. (CO2, K1) 2

2.c. Give the micro instruction format. (CO3, K1) 2

2.d. Define set associative mapping? (CO4, K2) 2

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2.e.	Define synchronous communication. (CO5, K1)	2

SECTION-B 30

3. Answer any five of the following:-

3-a.	Explain K-map with its variable types and diagram. (CO1, K3)	6
3-b.	Perform the 2's complement of 16 and give answer in binary format. (CO1, K3)	6
3-c.	Explain bus, list its types with proper diagram? (CO2, K1)	6
3-d.	Describe register with all its symbolic representation. (CO2, K1)	6
3.e.	Write down the operation of a control unit? (CO3, K1)	6
3.f.	Define Auxiliary memory with its characteristics? (CO4, K1)	6
3.g.	Differentiate Serial and Parallel communication interface. (CO5, K2)	6

SECTION-C 50

4. Answer any one of the following:-

4-a.	Explain Boolean Laws with example. (CO1, K1)	10
4-b.	Simplify the following functions F together with the don't care conditions d in (a) sum of products form and (b) product of sum form; F (w,x,y,z) = $\sum(0,1,2,3,7,8,10)$, d (w,x,y,z) = $\sum(5,6,11,15)$ (CO1, K3)	10

5. Answer any one of the following:-

5-a.	Define shift microoperation and also explain its types. (CO2, K2)	10
5-b.	Explain common bus system with example. (CO2, K2)	10

6. Answer any one of the following:-

6-a.	Explain stack organization with register and memory referencing. (CO3, K3)	10
6-b.	Explain how hardwired control unit is better than micro programmed, support your answer with example. (CO3, K2)	10

7. Answer any one of the following:-

7-a.	Explain set associative cache and dynamic RAM with example. (CO4, K2)	10
7-b.	Construct pyramid structure of memory hierarchy, explain each term. (CO4, K2)	10

8. Answer any one of the following:-

8-a.	Explain with suitable diagram and flowchart the process of data transfer from I/O device to CPU using the concept of programmed I/O. (CO5, K3)	10
8-b.	Explain how serial and parallel communication works with a help of diagram. (CO5, K2)	10