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Printed Page:-4 **Subject Code:- CEC0202**

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA
(An Autonomous Institute Affiliated to AKTU, Lucknow)
B.Tech
SEM: II - THEORY EXAMINATION (2025 - 2026)
Subject: Digital System Design

Time: 3 Hours **Max. Marks: 100**

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*
1. *This Question paper comprises of* ***three Sections -A, B, & C.*** *It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.*
2. *Maximum marks for each question are indicated on right -hand side of each question.*
3. *Illustrate your answers with neat sketches wherever necessary.*
4. *Assume suitable data if necessary.*
5. *Preferably, write the answers in sequential order.*
6. *No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.*

SECTION-A 20

1. Attempt all parts:-

(1.1) Which number system uses digits from 0 to 9 and letters A to F?(CO1 K1) 1

(a) Decimal
(b) Octal
(c) Hexadecimal
(d) Binary

(1.2) What is 1011_2 in decimal(CO1 K1) 1

(a) 10
(b) 11
(c) 12
(d) 13

(1.3) A half-adder circuit has two inputs and____ (CO2,K1) 1

(a) one output
(b) two output
(c) three output
(d) none of these

(1.4) A code converter is a logic circuit that _____(CO2,K1) 1

(a) Inverts the given input
(b) Converts into decimal number
(c) Converts data of one type into another type
(d) Converts to octal

(1.5) What is the set condition in an SR Latch?(CO3 K1) 1

(a) S=0,R=0
(b) S=1,R=0
(c) S=0,R=1
(d) S=1,R=1

(1.6) The SR latch is a type of: (CO3 K1) 1

(a) Asynchronus sequential circuit
(b) Synchronous sequential circuit
(c) Combinational cicuit
(d) Arithmetic circuit

(1.7) What happens to the parallel output word in an asynchronous binary down counter whenever a clock pulse occurs?.(CO4,K1) 1

(a) The output increases by 1
(b) The output decreases by 1
(c) The output word increases by 2
(d) The output word decreases by 2

(1.8) An asynchronous 4-bit binary down counter changes from count 2 to count 3. How many transitional states are required?.(CO4,K1) 1

(a) 1
(b) 2
(c) 8
(d) 15

(1.9) A PAL differs from a PLA in that PAL has:(CO5,K1) 1

(a) Both programmable AND and OR arrays
(b) Only programmable OR array
(c) Only programmable AND array
(d) Neither array programmable

(1.10) DRAM stores data using:(CO5,K1) 1

(a) Latches
(b) Capacitors
(c) MOSFET gates
(d) Magnetic cores

2. Attempt all parts:-

(2.1) Convert $(156)_{10}$ to binary, octal, and hexadecimal.(CO1 ,K1) 2

(2.2) Explain Half Subtractor.(CO2,K1) 2

(2.3) What is difference between latch and flip-flop? (CO3 K1) 2

(2.4) What is Excitation Table of Flip Flops?(CO4,K2) 2

(2.5) Define ROM.(CO5,K2) 2

SECTION-B 30

Answer any one of the following:-

(3.1) Simplify the Boolean expression using laws: A(B + A'C).(CO1 K2) 6

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(3.2)	Subtract 45 from 23 using 2's complement method.(CO1 K2)	6

Answer any one of the following:-

(3.3)	Explain full adder with proper logic circuit diagram. (CO2,K2)	6
(3.4)	Design 8:1 MUX by using 2:1. (CO2, K2)	6

Answer any one of the following:-

(3.5)	Describe the Race-around condition with suitable diagram, how to remove it? (CO3, K3)	6
(3.6)	With the help of neat logic diagram and function table, explain the working of a SR flip flop. (CO3, K3)	6

Answer any one of the following:-

(3.7)	What is synchronous counter? Explain its working with a 3-bit synchronous counter. (CO4, K3)	6
(3.8)	What is Hazard? Explain different type of Hazards. (CO4, K3).	6

Answer any one of the following:-

(3.9)	Compare RAM and ROM on the basis of speed, volatility, cost, storage and applications.(CO5,K3)	6
(3.10)	Compare PLA, PAL and PLD on the basis of flexibility, speed and cost.(CO5,K3)	6

SECTION-C 50

4. Answer any one of the following:-

(4.1)	Minimize the following logic function using K-maps and draw the logic circuit $F(A,B,C,D) = \Sigma m(1,3,5,8,9,11,15)+d(2,13)$ (CO1,K3)	10
(4.2)	Simplify the logic function F (W, X, Y, Z) = $\Sigma(1,3,7,11,15) + d(0,2)$ using K-map in SOP form and implement Using gate. (CO1,K3)	10

5. Answer any one of the following:-

(5.1)	Design a combinational circuit that will compare two 2-bit numbers.(CO2,K3)	10
(5.2)	Design Boolean function $F(A,B,C,D)= \sum m(0,2,5,6,8,11,12,13,15)$ by using 8:1 MUX . Choose B,C,D as select line.(CO2,K3)	10

6. Answer any one of the following:-

(6.1)	Describe the step-by-step process of converting an SR flip-flop into a JK flip-flop.(CO3, K4)	10
(6.2)	Explan the procedure to convert J-K flip-flop to T Flip-flop. Including conversion table (CO3, K4)	10

7. Answer any one of the following:-

(7.1)	Design Mod 4 synchronous counter using JK Flip-flop and implement it. (CO4, K4)	10
(7.2)	Design 3,4,1,0,2,5,6,7 Synchronous counter.(CO4,K4)	10

8. Answer any one of the following:-

(8.1)	A Combinational circuit is defined by the function $F1=\Sigma m(1,5,7)$ $F2= \Sigma m(5,6,7)$, Implement the circuit with a PLA. (CO5, K4)	10
(8.2)	Implement the given function in PAL, $A(w,x,y,z)= \Sigma m(0,2,6,7,8,9,12,13)$,$B(w,x,y,z)=$	10

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Σm(0,2,6,7,8,9,12,13,14),C(w,x,y,z)=Σm(1,3,4,6,10,12,13),Dw,x,y,z)=Σm(1,3,4,6,9,12,14) (CO5,K4)