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NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA
(An Autonomous Institute Affiliated to AKTU, Lucknow)

M.Tech

SEM: II - THEORY EXAMINATION (2025 - 2026)

Subject: Digital Design Using FPGA and CPLD

Time: 3 Hours

Max. Marks: 70

General Instructions:

IMP: Verify that you have received the question paper with the correct course, code, branch etc.

1. This Question paper comprises of **three Sections -A, B, & C**. It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.
2. Maximum marks for each question are indicated on right -hand side of each question.
3. Illustrate your answers with neat sketches wherever necessary.
4. Assume suitable data if necessary.
5. Preferably, write the answers in sequential order.
6. No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.

SECTION-A

15

1. Attempt all parts:-

- (1.1) How many different states does a 3bit asynchronous counter have? (CO1, K1) 1
- (a) 2
 - (b) 4
 - (c) 8
 - (d) 16
- (1.2) The change in state occurs during _____. (CO2, K2) 1
- (a) Pulse transition
 - (b) Outputs
 - (c) Input
 - (d) Clock Pulses
- (1.3) A PLA is similar to a ROM in concept except that- (CO3, K2) 1
- (a) It hasn't capability to read only
 - (b) It hasn't capability to read or write operation
 - (c) It doesn't provide full decoding to the variables
 - (d) It hasn't capability to write only
- (1.4) In FPGA, vertical and horizontal directions are separated by _____. (CO4, K2) 1
- (a) A line
 - (b) Channel
 - (c) Strobe
 - (d) Flip-Flop

- (1.5) CPLD stands for- (CO5, K1) 1
- (a) compute programmable Logic Devices
 - (b) Complex programmable Logic Devices
 - (c) Complex programmable Link Devices
 - (d) none of the above

2. Attempt all parts:-

- (2.1) What will be the output for the expression $Z = A \text{ XOR } B$, when $A=1$ and $B=0$. (CO1, K2) 2
- (2.2) How does hazard occur? (CO2, K2) 2
- (2.3) Differentiate between PLA and ROM. (CO3, K4) 2
- (2.4) Discuss Course Grain FPGA Technology? (CO4, K3) 2
- (2.5) Discuss Cascade Chain Operation. (CO5, K3) 2

SECTION-B

20

Answer any one of the following:-

- (3.1) Discuss various types of state machine. (CO1, K3) 4
- (3.2) Draw the Moore state diagram for the 101 sequence detector. (CO1, K5) 4

Answer any one of the following:-

- (3.3) How race condition can be avoided in a flip flops? (CO2, K2) 4
- (3.4) Give the design Procedure for asynchronous sequential circuit. (CO2, K4) 4

Answer any one of the following:-

- (3.5) Draw the general structure of PAL. (CO3, K5) 4
- (3.6) What do you mean by the term volatile memory? Discuss with the help of an example. (CO3, K3) 4

Answer any one of the following:-

- (3.7) Discuss Input-output Block Related to FPGA. (CO4, K3) 4
- (3.8) Draw & explain various Logic block of FPGA. (CO4, K5) 4

Answer any one of the following:-

- (3.9) Give some differences between FPGA and CPLDs with diagram. (CO5, K4) 4
- (3.10) Explain Altera MAX 5000 series Programmable Interconnect Array. (CO5, K2) 4

SECTION-C

35

4. Answer any one of the following:-

- (4.1) Design the circuit for 2 bit Up counter starting from the Moore FSM. (CO1, K5) 7
- (4.2) Draw the Mealy state diagram and the corresponding ASM chart for the 0111 sequence detector, if repetition is allowed. (CO1, K5) 7

5. Answer any one of the following:-

- (5.1) What do you mean by hazards? Explain Essential hazards and functional hazards in detail. (CO2, K2) 7
- (5.2) Design a serial adder using a full adder and a flip flop. (CO2, K5) 7

6. Answer any one of the following:-

- (6.1) What do you understand by the ROM? Discuss in detail about NAND based ROM.(CO3, K3) 7
- (6.2) Elaborate Read and Write operation of NOR based ROM. (CO3, K3) 7
7. Answer any one of the following:-
- (7.1) Discuss in detail FPGA design flow.(CO4, K3) 7
- (7.2) How would you implement a binary counter using the CLBs of FPGA? (CO4, K2) 7
8. Answer any one of the following:-
- (8.1) Implement any 5- variable Boolean expression using Cypress FLASH 370 CPLDs with diagram. (CO5, K5) 7
- (8.2) Describe in detail ALTERA FLEX 10K Logic Array Block. (CO5, K2) 7

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