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NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA
(An Autonomous Institute Affiliated to AKTU, Lucknow)

M.Tech

SEM: II - THEORY EXAMINATION (2025 - 2026)

Subject: Low Power VLSI Design

Time: 3 Hours

Max. Marks: 70

General Instructions:

IMP: Verify that you have received the question paper with the correct course, code, branch etc.

1. This Question paper comprises of **three Sections -A, B, & C**. It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.

2. Maximum marks for each question are indicated on right -hand side of each question.

3. Illustrate your answers with neat sketches wherever necessary.

4. Assume suitable data if necessary.

5. Preferably, write the answers in sequential order.

6. No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.

SECTION-A

15

1. Attempt all parts:-

- (1.1) In CMOS logic circuit the n-MOS transistor acts as:(CO1,K3) 1
- (a) Load
- (b) Pull up network
- (c) Pull down network
- (d) Not used in CMOS circuits
- (1.2) The electrical behaviour of a circuit is given using _____. (CO2,K4) 1
- (a) Design rules
- (b) Floor plan
- (c) Structures and layouts
- (d) Mathematical modelling
- (1.3) The flip-flop is only activated by _____(CO3,k2) 1
- (a) Positive edge trigger
- (b) Negative edge trigger
- (c) Either positive or Negative edge trigger
- (d) Sinusoidal trigger
- (1.4) A combinational circuit that selects one from many inputs are _____(CO4,k3) 1
- (a) Encoder
- (b) Decoder
- (c) Demultiplexer
- (d) Multiplexer

- (1.5) In negative logic convention, the Boolean Logic [1] is equivalent to: (CO5,K2) 1
- (a) +VDD
 - (b) 0 V
 - (c) -VDD
 - (d) None of the mentioned

2. Attempt all parts:-

- (2.1) Explain W/ L ratio? (CO1,K2) 2
- (2.2) What is short circuit power? (CO2,K2) 2
- (2.3) Explain the importance of Gray Code? (CO3,K2) 2
- (2.4) Why is SRAM expensive? (CO4,K3) 2
- (2.5) How the propagation delay get affected by increasing fanout? (CO5,K3) 2

SECTION-B

20

Answer any one of the following:-

- (3.1) Explain the transistor sizing. (CO1,K2) 4
- (3.2) Draw the fabrication steps of NMOS transistor and explain its operation in detail. (CO1,K2) 4

Answer any one of the following:-

- (3.3) Explain in detail switch off clock signal? (CO2,K2) 4
- (3.4) Explain suitable leakage reduction techniques. (CO2,K2) 4

Answer any one of the following:-

- (3.5) What is latch-up condition in CMOS circuits? How it can be eliminated. (CO3,K2) 4
- (3.6) What is race around condition? How to eliminate race around condition? (CO3,K3) 4

Answer any one of the following:-

- (3.7) What are the objectives of performance management, explain? (CO4,K2) 4
- (3.8) What is the disadvantage of ripple carry adder? Explain with logic diagram. 4

Answer any one of the following:-

- (3.9) What is multiplexer? Explain with the help of circuit diagram. (CO5,K2) 4
- (3.10) Explain the issues involved in low power clock distribution? (CO5,K2) 4

SECTION-C

35

4. Answer any one of the following:-

- (4.1) Write short note on 'impact of technology Scaling'. (CO1,K3) 7
- (4.2) Explain parasitic capacitance with the help of diagram. (CO1,K2) 7

5. Answer any one of the following:-

- (5.1) Explain probabilistic power estimation approaches. (CO2,K2) 7
- (5.2) What is subthreshold leakage current? Explain with circuit diagram. (CO2,K2) 7

6. Answer any one of the following:-

- (6.1) Explain briefly the difference between the Mealy model and Moore model. (CO3,K3) 7

- (6.2) Explain the operation of Master Slave JK flip flop. (CO3,K2) 7
7. Answer any one of the following:-
- (7.1) Draw and explain the operation of 6 transistor SRAM. (CO4,k2) 7
- (7.2) What is Flow Graph Transformation? Explain in details. (CO4,K2) 7
8. Answer any one of the following:-
- (8.1) What is CMOS? Implement CMOS circuit of given boolean expression $Y=(ab+c+d)'$. (CO5,K4) 7
- (8.2) Write short note on zero skew chip Vs tolerable skew chip.(CO5,K3) 7

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