.

Printed Page:-3 **Subject Code:- AMTVL0211**

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA
(An Autonomous Institute Affiliated to AKTU, Lucknow)
M.Tech
SEM: II - THEORY EXAMINATION (2025 - 2026)
Subject: VLSI Testing and Testability

Time: 3 Hours **Max. Marks: 70**

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*
1. *This Question paper comprises of* ***three Sections -A, B, & C.*** *It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.*
2. *Maximum marks for each question are indicated on right -hand side of each question.*
3. *Illustrate your answers with neat sketches wherever necessary.*
4. *Assume suitable data if necessary.*
5. *Preferably, write the answers in sequential order.*
6. *No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.*

SECTION-A 15

1. Attempt all parts:-

(1.1) ATPG stands for_____.(CO1,K1) 1

(a) Attenuated Transverse wave Pattern Generation
(b) Automatic Test Pattern Generator
(c) Aligned Test Parity Generator
(d) None of these

(1.2) Test generation effort for n gate circuit is proportional to _____.(CO2,K2) 1

(a) n
(b) n2
(c) n3
(d) n2 and n3

(1.3) The full form of LSSD. (CO3,K2) 1

(a) Level scan sub design
(b) Level sensitive scan design
(c) Level sensitive sub design
(d) none of these

(1.4) IDDQ fault occurs when there is (CO4,K2) 1

(a) increased voltage
(b) increased quiescent current
(c) increased power supply
(d) increased discharge

(1.5) Which method has more area overhead?(CO5,K2) 1

(a) random test pattern
(b) pseudo random test pattern
(c) algorithimic test pattern
(d) deterministic test pattern

2. Attempt all parts:-

(2.1)	What are the differences between online and offline testing? (CO1,K2)	2
(2.2)	Explain single path sensitization. (CO2,K2)	2
(2.3)	What is the objective of scan design technique?(CO3,K2)	2
(2.4)	Write the name of RAM coupling faults.(CO4,K2)	2
(2.5)	What are the difficulties in psuedo random testing? (CO5,K2)	2

SECTION-B 20

Answer any one of the following:-

(3.1)	Differentiate single stuck and multiple stuck at fault models. (CO1,K3)	4
(3.2)	Write some of the applications of fault simulation. (CO1,K2)	4

Answer any one of the following:-

(3.3)	With the help of a good example explain fault activation and fault propagation.(CO2,K3)	4
(3.4)	Explain the forward and backward implications.(CO2,K2)	4

Answer any one of the following:-

(3.5)	Write the things that should be followed in ad-hoc DFT methods.(CO3,K2)	4
(3.6)	What are the requirements for scan design?(CO3,K3)	4

Answer any one of the following:-

(3.7)	Explain the procedure for detecting the bridging fault by IDDQ testing.(C04,K2)	4
(3.8)	Discuss the limitations of IDDQ testing.(CO4,K2))	4

Answer any one of the following:-

(3.9)	With the help of good example discuss the differences between pseudo exhaustive test generation and pseudo random test generation methods.(CO5,K3)	4
(3.10)	List the memory test requirements for Memory BIST.(CO5,K2)	4

SECTION-C 35

4. Answer any one of the following:-

(4.1)	What is functional testing? Why functional testing is difficult to be performed on a complex circuit?(CO1,K1)	7
(4.2)	Explain in detail the external representation and internal representation in structural models of VLSI circuits.(CO1,K2)	7

5. Answer any one of the following:-

(5.1)	Discuss about the test generation basics and explain the random test generation with suitable diagram. (CO2,K2)	7
(5.2)	With the help of suitable example explain the D algorithm in detail.(CO2,K3)	7

6. Answer any one of the following:-

.

(6.1)	Discuss the differences between combinational and sequential testing.Explain with example.(CO3,K3)	7
(6.2)	Describe a full scan structure implemented in a digital design. What are the scan overheads? (CO3,K2)	7

7. Answer any one of the following:-

(7.1)	With neat diagrams explain different types of memory and Key Issues in Memory Integration. (CO4,K3)	7
(7.2)	Explain Memory chip test algorithms with suitable example.(CO4,K2)	7

8. Answer any one of the following:-

(8.1)	How a built-in-self test is classified? Give some examples.(CO5, K4)	7
(8.2)	Draw the block diagram for a BIST implementation using BILBO and explain the test procedure.(CO5,K4)	7