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**Printed Page:-3** **Subject Code:- AMTVL0215**

**Roll. No:**

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**NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA**
**(An Autonomous Institute Affiliated to AKTU, Lucknow)**
**M.Tech**
**SEM: II - THEORY EXAMINATION (2025 - 2026)**
**Subject: Nanoscale Devices: Modeling &Simulation**

**Time: 3 Hours** **Max. Marks: 70**

**General Instructions:**

**IMP:** *Verify that you have received the question paper with the correct course, code, branch etc.*
***1.*** *This Question paper comprises of* ***three Sections -A, B, & C.*** *It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.*
***2.*** *Maximum marks for each question are indicated on right -hand side of each question.*
***3.*** *Illustrate your answers with neat sketches wherever necessary.*
***4.*** *Assume suitable data if necessary.*
***5.*** *Preferably, write the answers in sequential order.*
***6.*** *No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.*



## SECTION-A 15

1. Attempt all parts:-

(1.1) If the depletion-layer widths (xdS, xdD) of the source and drain junction and L is Channel length then In DIBL case. (CO1,K2) 1

(a) xdS + xdD = L
(b) xdS + xdD > L
(c) xdS + xdD < L
(d) xdS - xdD < L

(1.2) The bulk charge (QB),is generated due to , (CO2,K2) 1

(a) the depletion of majority carriers
(b) the depletion of minority carriers
(c) due to inversion layers of mobile carriers
(d) None of these

(1.3) In Twin Silicon Nanowire FET, gate stack is of number ____ (CO3,K2) 1

(a) 1
(b) 2
(c) 3
(d) 4

(1.4) FinFET was developed to overcome the....(CO4,K2) 1

(a) short-channel effect
(b) large-channel effect
(c) mid-channel effect
(d) no channel effect

(1.5) Why is SRAM more preferably in non-volatile memory? (CO5,K2) 1

(a) low-cost
(b) high-cost
(c) low power consumption
(d) transistor as a storage element

2. Attempt all parts:-

(2.1) What is small geometry effect? (CO1,K2) 2

(2.2) What is the threshold voltage? Write formula for the drain current and thresold voltage. (CO2,K3) 2

(2.3) Why CNTFETs is better than conventional Mosfet? (CO3,K2) 2

(2.4) What are the thermal issues in a SOI devices? (CO4,K2) 2

(2.5) Which is the fastest ADC? State the reason. (CO5,K3) 2

**SECTION-B** 20

Answer any<u>one</u> of the following:-

(3.1) What is Parcially depleted SOI ? What are the advantage of PDSOI ? (CO1,K2) 4

(3.2) What is Gate Induced Drain Leakage (GIDL) ? How its generated ? (CO1,K2) 4

Answer any<u>one</u> of the following:-

(3.3) Explain the oxide thickness effect in detail with suitable diagram.(CO2,K3) 4

(3.4) What is Miller overlap capacitance ? How it measured? (CO2,K2) 4

Answer any<u>one</u> of the following:-

(3.5) What is Nano transistor? How do Nano transistor Work? (CO3,K3) 4

(3.6) Explain any four applications of semiconductor nanowire FETs. (CO3,K2) 4

Answer any<u>one</u> of the following:-

(3.7) Discuss the body effect in CMOS devices. (CO4,K2) 4

(3.8) Enlist the advantage and Disadvantage GAA technology. (CO4,K2) 4

Answer any<u>one</u> of the following:-

(3.9) Explain in brief the principle of operation of successive Approximation ADC. (CO5,K3) 4

(3.10) What are the advantages and disadvantages of SAR ADC? (CO5,K2) 4

**SECTION-C** 35

4. Answer any <u>one</u> of the following:-

(4.1) What do you mean by drain punch through condition? Explain it with suitable diagram.(CO1,K3) 7

(4.2) How to deal with Parasitic Capacitance in MOSFET? How its degrade the performance of MOSFET? (CO1,K2) 7

5. Answer any <u>one</u> of the following:-

(5.1) What is quantum-mechanical approach in Electron concentration distribution? Explain in detail (CO2,K3) 7

(5.2) Disscuss Symmetrical operation of DGSOI FETs with suitable diagram. (CO2,K3) 7

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6. Answer any one of the following:-

| | | |
|---|---|---|
| (6.1) | What is Carbon Nano Tube? Discuss the Top-down and Bottom-up approach for creating nanostructures with suitable diagram. (CO3,K3) | 7 |
| (6.2) | Discuss the energy band diagram of CNTFETs and define LUMO and HOMO in semiconductor? (CO3,K3) | 7 |

7. Answer any one of the following:-

| | | |
|---|---|---|
| (7.1) | Why switch to FD-SOI at next CMOS nodes, and what are the key advantages of FD-SOI? (CO4,K2) | 7 |
| (7.2) | How total ionizing dose effects works in single-gate SOI? Explain in detail with suitable diagram (CO4,K3) | 7 |

8. Answer any one of the following:-

| | | |
|---|---|---|
| (8.1) | How LC-VCO can be used in RF circuit. Explain in detail? (CO5,K2) | 7 |
| (8.2) | What are the advantages and disadvantages of op-amp? Write it applications in nanoelectronics. (CO5,K3) | 7 |