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Printed Page:-4 **Subject Code:- BEC0402N**

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA
(An Autonomous Institute Affiliated to AKTU, Lucknow)
B.Tech
SEM: IV - THEORY EXAMINATION (2025 - 2026)
Subject: Microprocessor & Microcontroller

Time: 3 Hours **Max. Marks: 100**

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*

1. *This Question paper comprises of* ***three Sections -A, B, & C.*** *It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.*

2. *Maximum marks for each question are indicated on right -hand side of each question.*

3. *Illustrate your answers with neat sketches wherever necessary.*

4. *Assume suitable data if necessary.*

5. *Preferably, write the answers in sequential order.*

6. *No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.*

SECTION-A 20

1. Attempt all parts:-

(1.1) In Von Neumann architecture, instructions and data share the same_____. (CO1,K1) 1

(a) ALU
(b) register
(c) memory and bus
(d) cache only

(1.2) RISC stands for_____. (CO1,K1) 1

(a) Reduced Instruction Set Computer
(b) Rapid Instruction Set Computer
(c) Real Instruction Set Computer
(d) Random Instruction Set Computer

(1.3) The size of the 8086 address bus is -------. (CO2,K1) 1

(a) 16-bit
(b) 20-bit
(c) 32-bit
(d) 8-bit

(1.4) The size of the flag register in 8086 is ___. (CO2,K1) 1

(a) 8-bit
(b) 16-bit
(c) 20-bit
(d) 32-bit

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(1.5) Each port in 8051 is of_____. (CO3,K1) 1

(a) 4 bits
(b) 8 bits
(c) 16 bits
(d) 32 bits

(1.6) PSW stands for_____: (CO3,K1) 1

(a) Program Status Word
(b) Processor Status Word
(c) Program Stack Word
(d) None

(1.7) Number of general-purpose registers in Cortex-M0 is ---------. (CO4,K1) 1

(a) 13
(b) 16
(c) 8
(d) 32

(1.8) Cortex-M0 memory map size is----. (CO4,K1) 1

(a) 4GB
(b) 1GB
(c) 2GB
(d) 8GB

(1.9) POP instruction is used for_____. (CO5,K2) 1

(a) Stack read
(b) Stack write
(c) Shift
(d) Rotate

(1.10) ADD instruction performs _____. (CO5,K1) 1

(a) Addition
(b) Subtraction
(c) Multiplication
(d) Division

2. Attempt all parts:-

(2.1) Write the basic difference between a microprocessor and a microcontroller. (CO1,K2) 2

(2.2) Define Execution Unit (EU). (CO2,K2) 2

(2.3) State the difference between direct and indirect addressing modes. (CO3,K2) 2

(2.4) List any two ARM processor families. (CO4,K1) 2

(2.5) Define MOV instruction in ARM. (CO5,K2) 2

SECTION-B 30

Answer any one of the following:-

(3.1) Explain the historical development of microprocessors and microcontrollers, 6

highlighting major technological milestones and their impact on modern computing. (CO1,K3)

(3.2) Discuss memory organization in microprocessor systems and explain the interaction between CPU, memory, and I/O devices. (CO1,K3) 6

Answer any one of the following:-

(3.3) Describe the functions of Bus Interface Unit and Execution Unit in detail. (CO2,K2) 6

(3.4) Discuss the structure and function of flag register in 8086. (CO2,K3) 6

Answer any one of the following:-

(3.5) Explain the architecture of 8051 microcontroller with its major components. (CO3,K3) 6

(3.6) Describe the data types used in 8051 programming. (CO3,K2) 6

Answer any one of the following:-

(3.7) Explain the ARM processor family classification and their application areas. (CO4,K3) 6

(3.8) Describe the block diagram of Cortex-M0 and explain each functional unit. (CO4,K3) 6

Answer any one of the following:-

(3.9) Explain three stage pipelining in Cortex-M0 with proper diagram. (CO5,K3) 6

(3.10) Explain the role of ALU in ARM processor. (CO5,K3) 6

SECTION-C 50

4. Answer any one of the following:-

(4.1) Analyze the fundamental differences between RISC and CISC architectures with respect to instruction complexity, execution cycle, hardware design, power efficiency, and software support. (CO1,K3) 10

(4.2) Discuss the concept of pipelining in processor architecture and analyze its benefits and limitations. (CO1,K3) 10

5. Answer any one of the following:-

(5.1) Explain different addressing modes of 8086 with suitable examples. (CO2.K3) 10

(5.2) Describe the pin diagram of 8086 and explain signals in minimum and maximum mode. (CO2,K3) 10

6. Answer any one of the following:-

(6.1) Classify the 8051 instruction set and explain each category. (CO3,K3) 10

(6.2) Explain various arithmetic and logical instructions of 8051 with examples. (CO3,K3) 10

7. Answer any one of the following:-

(7.1) Discus the register organization of Cortex-M0. (CO4,K3) 10

(7.2) Explain the concept of endianness in Cortex-M0 with examples. (CO4,K3) 10

8. Answer any one of the following:-

(8.1) Explain instruction set architecture of Cortex-M0 and analyze its efficiency. (CO5,K3) 10

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(8.2) Explain pipeline hazards and discuss techniques to handle them in Cortex-M0. (CO5,K4) 10