Printed page: 4 Subject Code: BEC0403

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NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

B.Tech

SEM: IV - THEORY EXAMINATION (2025-2026)

Subject -CMOS Digital Integrated Circuit

Time: 3 Hours **Max. Marks:100**

General Instructions:

IMP: Verify that you have received question paper with correct course, code, branch etc.

1. *This Question paper comprises of three Sections -A, B, & C. It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.*
2. *Maximum marks for each question are indicated on right hand side of each question.*
3. *Illustrate your answers with neat sketches wherever necessary.*
4. *Assume suitable data if necessary.*
5. *Preferably, write the answers in sequential order.*
6. *No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.*

SECTION – A 20

1. Attempt all parts:-

(1.1) Latch-up in CMOS circuits is mainly caused due to: (CO1,K3) 1

(a) High switching speed

(b) Parasitic bipolar transistor action

(c) Low supply voltage

(d) High threshold voltage

(1.2) In an n-well CMOS process, PMOS transistors are fabricated in:(CO1,K2) 1

(a) p-substrate

(b) n-well

(c) oxide layer

(d) polysilicon layer

(1.3) The switching threshold (Vm) of a CMOS inverter is ideally: (CO2,K1) 1

(a) 0

(b) VDD

(c) VDD/2

(d) Depends only on load

(1.4)	Propagation delay in a CMOS inverter depends primarily on: (CO2,K3) (a) Temperature only (b) Load capacitance and transistor size (c) Input frequency only (d) Substrate bias only	1
(1.5)	An edge-triggered flip-flop changes state: (CO3,K2) (a) At logic high level (b) At logic low level (c) Only at clock transitions (d) Randomly	1
(1.6)	Which CMOS logic family uses less power but operates at higher speeds? (CO3,K3) (a) Static CMOS (b) Dynamic CMOS (c) Pass transistor logic (d) BiCMOS	1
(1.7)	In Domino Logic, evaluation occurs during: (CO4,K1) (a) Precharge phase (b) Evaluation phase (c) Idle phase (d) Reset phase	1
(1.8)	Pass Transistor Logic primarily reduces: (CO4,K3) (a) Power consumption (b) Number of transistors (c) Noise margin (d) Delay time	1
(1.9)	In ASIC design flow, placement refers to: (CO5,K1) (a) Connecting wires (b) Positioning circuit components on chip (c) Testing the chip (d) Fabricating transistors	1
(1.10)	Which memory requires periodic refreshing? (CO5,K2) (a) SRAM (b) DRAM (c) ROM (d) Flash	1

2. Attempt all parts:-

(2.1)	What is latch-up in CMOS circuits? (CO1,K3)	2
(2.2)	Define noise margins in a CMOS inverter. (CO2,K1)	2
(2.3)	How can Boolean expressions be realized using CMOS logic gates? (CO3,K3)	2
(2.4)	Mention advantages of Domino logic over static CMOS logic. (CO4,K1)	2
(2.5)	What are lambda-based design rules in VLSI layout design? (CO5,K2)	2

SECTION – B 30

Answer any <u>one</u> of the following-

(3.1)	Calculate the drain current (Id) of a MOSFET operating in saturation given:$V_{GS} = 2V, V_{th} = 1V, \mu_n C_{ox} = 50\mu A/V^2, W/L = 10$. (CO1,K4)	6
(3.2)	Explain the VLSI design flow in detail. Illustrate the role of each stage from system specification to fabrication. (CO1,K2)	6

Answer any <u>one</u> of the following-

(3.3)	Explain the operation of CMOS inverter with voltage transfer characteristics (VTC). (CO2,K2)	6
(3.4)	Determine switching threshold V_M for given PMOS and NMOS parameters. (CO2,K2)	6

Answer any <u>one</u> of the following-

(3.5)	Explain the operation of D latch with timing diagram. (CO3,K2)	6
(3.6)	Design a full adder using CMOS logic.Write the equation for outputs sum and carry. (CO3,K2)	6

Answer any <u>one</u> of the following-

(3.7)	Explain clock distribution challenges in VLSI circuits. (CO4,K2)	6
(3.8)	Explain dynamic CMOS logic and its advantages over static CMOS. (CO4,K2)	6

Answer any <u>one</u> of the following-

(3.9)	Compare SRAM and DRAM and give their applications. (CO5,K3)	6
(3.10)	Explain the different abstraction levels in VLSI design methodology, including behavioral, structural, and physical levels. (CO5,K2)	6

SECTION – C 50

4. Answer any <u>one</u> of the following-

(4.1)	Derive the basic MOSFET current-voltage equations and explain the operation of MOS transistor as a switch. Include the effect of threshold voltage and channel length. (CO1,K4)	10
(4.2)	Draw the energy band diagram for MOS structure for three regions of operation and explain why band bending is there at the surface? (CO1,K4)	10

5. Answer any one of the following-

(5.1)	Consider a CMOS inverter circuit with the following parameters: V DD =3 .3V, V Tn =0.6 V, V TP = -0.7 V, kn= 200 uA/V^2, kp = 80 uA/V^2. Calculate the noise margins of the circuit. (CO2,K4)	10
(5.2)	Design a 2:1 multiplexer using CMOS logic and explain its operation. Discuss its importance in digital systems. (CO2,K6)	10

6. Answer any one of the following-

(6.1)	Design a 2-input CMOS NAND gate and verify its truth table.(CO3,K3)	10
(6.2)	Explain pass transistor logic and compare it with transmission gate logic in terms of performance and reliability. (CO3,K3)	10

7. Answer any one of the following-

(7.1)	Design a domino logic circuit for OR gate. Discuss its advantages and challenges. (CO4,K2)	10
(7.2)	Discuss clock distribution and clocking issues in high-performance VLSI systems. How do they affect synchronization? (CO4,K3)	10

8. Answer any one of the following-

(8.1)	Explain the ASIC design flow, focusing on backend processes such as floorplanning, placement, routing, and verification.(CO5,K2)	10
(8.2)	Discuss testing and verification techniques used in ASIC design to ensure reliability and manufacturability. (CO5,K2)	10