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Printed Page:-3 **Subject Code:- BEC0613**

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA
(An Autonomous Institute Affiliated to AKTU, Lucknow)
B.Tech
SEM: VI - THEORY EXAMINATION (2025 - 2026)
Subject: VLSI Testing and Reliability

Time: 3 Hours **Max. Marks: 100**

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*
1. *This Question paper comprises of* ***three Sections -A, B, & C.*** *It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.*
2. *Maximum marks for each question are indicated on right -hand side of each question.*
3. *Illustrate your answers with neat sketches wherever necessary.*
4. *Assume suitable data if necessary.*
5. *Preferably, write the answers in sequential order.*
6. *No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.*

SECTION-A 20

1. Attempt all parts:-

(1.1) What is the main objective of testing in VLSI circuits? (CO1,K1) 1

(a) Increase power consumption
(b) Detect manufacturing defects
(c) Reduce chip size
(d) Improve packaging

(1.2) Which testing is used to verify the functionality of a circuit at logic level? (CO1,K1) 1

(a) Functional testing
(b) Packaging test
(c) Burn-in test
(d) Visual inspection

(1.3) Boolean difference method is used to determine. (CO2,K1) 1

(a) Chip size
(b) Fault detectability
(c) Power usage
(d) Package type

(1.4) D-algorithm is mainly used for: (CO2,K1) 1

(a) ATPG
(b) Burn-in testing
(c) Functional simulation
(d) Packaging

(1.5) Sequential circuit testing is often converted into: (CO3,K1) 1

(a) Analog testing
(b) Iterative combinational testing
(c) Packaging testing
(d) Burn-in testing

(1.6) Design for testability in sequential circuits improves: ((CO3,K1) 1

(a) Controllability and observability
(b) Chip size only
(c) Package strength
(d) Wafer thickness

(1.7) BIST stands for: (CO4,K1) 1

(a) Basic Internal System Test
(b) Built-In Self-Test
(c) Binary Integrated System Test
(d) Built-In Signal Test

(1.8) The main purpose of BIST is to: ((CO4,K1) 1

(a) Increase chip size
(b) Improve packaging
(c) Reduce testing cost
(d) Reduce power only

(1.9) UVM stands for: (CO5,K1) 1

(a) Unified Verification Method
(b) Universal Verification Methodology
(c) User Verification Model
(d) Universal Virtual Method

(1.10) DUT stands for: (CO5,K1) 1

(a) Data Unit Test
(b) Device Under Test
(c) Design Utility Tool
(d) Digital Unit Tool

2. Attempt all parts:-

(2.1) Define testing in VLSI circuits. (CO1,K1) 2

(2.2) Define Boolean difference. (CO2,K2) 2

(2.3) Define state table verification. (CO3,K2) 2

(2.4) Explain BIST with the help of its block diagram. (CO4,K2) 2

(2.5) Define UVM. (CO5,K1) 2

SECTION-B 30

Answer any one of the following:-

(3.1) Explain the principle of testing in VLSI circuits. (CO1,K2) 6

(3.2) Discuss the testing flow from wafer test to final test. (CO1,K2) 6

Answer any one of the following:-

(3.3)	Explain path sensitization with an example. (CO2,K2)	6
(3.4)	Describe Boolean difference method for test generation. (CO2,K2)	6

Answer any one of the following:-

(3.5)	Explain testing of sequential circuits as iterative combinational circuits. (CO3,K3)	6
(3.6)	Explain test generation based on circuit structure. (CO3,K3)	6

Answer any one of the following:-

(3.7)	Explain BIST architecture for a testing a sequential logic circuit. (CO4,K3)	6
(3.8)	Describe the function of Output Response Analysis (ORA). (CO4,K2)	6

Answer any one of the following:-

(3.9)	Write short notes on RAL and TLM in UVM. (CO5,K2)	6
(3.10)	Describe the role of transactions in UVM verification. (CO5,K2)	6

SECTION-C 50

4. Answer any one of the following:-

(4.1)	Explain the principle of VLSI testing and discuss different types of testing in detail. (CO1,K3)	10
(4.2)	Discuss DC and AC parametric tests with suitable examples and comparisons. (CO1,K3)	10

5. Answer any one of the following:-

(5.1)	Explain test generation algorithms and discuss different methods used in combinational circuit testing. (CO2,K3)	10
(5.2)	Explain D-algorithm in detail and describe its role in ATPG for combinational circuits. (CO2,K3)	10

6. Answer any one of the following:-

(6.1)	Explain testing of sequential circuits using iterative combinational models in detail. (CO3,K3)	10
(6.2)	Discuss state table verification and structural test generation methods for sequential circuits. (CO3,K3)	10

7. Answer any one of the following:-

(7.1)	Explain test pattern generation in BIST and discuss different BIST architectures in detail. (CO4,K3)	10
(7.2)	Describe delay faults and delay testing methods used in VLSI circuits. (CO4,K3)	10

8. Answer any one of the following:-

(8.1)	Explain Universal Verification Methodology (UVM) and discuss its advantages over traditional verification methods. (CO5,K3)	10
(8.2)	Explain the UVM architecture with suitable diagram also the UVM phases. (CO5,K3)	10