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Title: A distinct carry celect adder design approach for area and delay reduction using modified full adder

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ABSTRACT: A SQRT Carry Select Adder (CSLA) design with modified full adder architecture is proposed in this work. The regular SQRT CSLA has less delay but it is bulky when compared with other adders. The proposed design has reduced area and delay for a SQRT CSLA. The architecture is designed for a 128bit and is synthesized, simulated in Vivado v2017.2 software. The result concludes that the new design is giving a considerable amount of reduction in area and delay. Also, the proposed design is of 128-bit therefore it can be used in the future designs of efficient processor.

Keywords: Carry select adder; Full adder; Linear CSLA multiplexer based full adder; SQRT CSLA

I. INTRODUCTION

In the digital signal processing (DSP) adders have higher precedence. Adders are the basic blocks of the digital signal processing chips and are of different types. The different types of digital adders includes ripple carry adder (RCA), carry skip adder (CSKA), carry look ahead adder (CLA), carry increment adder (CIA), carry save adder (CSA) and carry select adder (CSLA). Among all the digital adders CSLA has a higher speed [1]. In RCA the carry from the starting stage is rippled to the remaining stages. This increases the propagation delay and the output sum appears only when the carry reaches the particular stage. The delay in RCA is increased linearly with the size of the input bits.

In all the adders propagation of carry and gate count in the propagation path are the major cause for delay. An efficient architecture that reduces the delay due to the

propagation of the carry is the CSLA. Bedrij proposed that the difficulty of carry transition delay is rectified by generation of multiple radix carries and simultaneously generated sums are selected by using these carries [2]. In CSLA the sum output is generated even before the carry from previous stages is generated. The structure of CSLA generates the sum output for C_{in} = 1 and C_{in} = 0 also and the multiplexer is provided with the output carry from the preceding stages. Regular CSLA has linear bit grouping unlike the SQRT CSLA which has non-linear bit grouping [3-7]. In CSLA the delay is reduced by pre-computing the output sum without the arrival of carry. The area consumed by the conventional CSLA is high compared with the other types of adders. The gate count and area are reduced by using a binary to excess-one code converter (BEC), the BEC is used to replace the RCA structure used for generating the sum output when carry from the previous stage is one [8–9]. To reduce the area consumption of CSLA further, the 1-bit full adders in the RCA are designed with multiplexers.

The multiplexer based full adder consumes less area when compared with the other conventional designs of the full adder because of only two transistors are required to implement a multiplexer. The proposed design has a full adder that is entirely designed using six multiplexers. The rest of the paper is organized as follows section II introduces the proposed architecture details. Section III elaborates the simulation results and comparisons. Section IV concludes the work.

II. PROPOSED METHODOLOGY:

The functioning of CSLA can be comprehended by analyzing it in three distinct stages. 1. Ripple carry adder, 2. Full Adders, and 3. Multiplexers.

A 4-bit RCA is shown in the Figure 1. The RCA of 4bit is developed with 4 full adders (1-bit) connected in cascaded form. The RCA of K input bits is implemented with K full adder structures. An output of (K + 1) bits is generated from a K-bit RCA and 8 OR gates. Since the implementation ofthe EX-OR gate requires a minimum of 12 transistors the area consumption is high when used excessively.

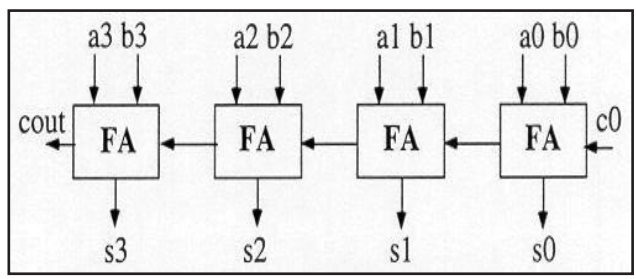

Figure 1. A 4-bit ripple carry adder using 4 full adders [2]

The multiplexers used in the CSLA design depends on the number of bits given to the RCA of the corresponding multiplexer. The sum output is chosen by the multiplexer between the responses of the RCA-1 and RCA-2 depending on the position of the C_{in}. When the C_{in} = 1 RCA-2 output is chosen as the sum and when C_{in} = 0 the response from the RCA-1 is considered by the multiplexer. The full adders used in the existing design are modified by the modified full adder structure. The modified full adder structure is given in Figure 3. It contains six 2:1 multiplexers for generating sum and carry. Since a multiplexer requires only 2 transistors, the area consumed by the designed adder is reduced by nearly 5% than the existing design. The comparison data can be viewed in TABLE 1. The full adder responses are the sum and carry, they are given in Boolean form as follows.

$$SUM = X_0 \oplus X_1 \oplus X_2 \quad (1)$$

$$CARRY = X_0.X_1 + X_1.X_2 + X_2.X_0 \quad (2)$$

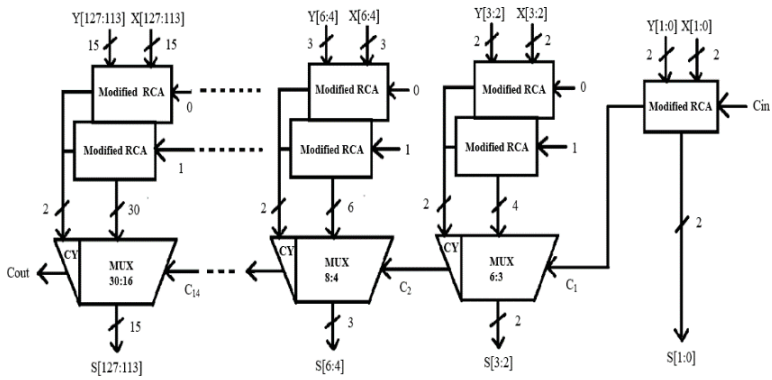

Figure 2. Proposed 128-bit CSLA design using modified full adder

III. RESULTS

This proposed work is done in Verilog-HDL and simulated using the Xilinx Vivado 2017.2 software, the results of our modified full adder based design and the regular adder design are depicted in Figure 5 and Figure 6 respectively. The comparison of the area required by the regular 128-bit SQRT CSLA and our modified 128-bit SQRT CSLA is shown in Table I.

Table I. Comparison of area and delay of normal full adder based and modified full adder based structures

Adders name	**Total number of LUTs consumed**	**Total delay**	
		Setup	***Hold***
Normal full adder based SQRT CSLA	270	5.984 ns	0.34 ns
Modified full adder based SQRT CSLA	246	5.662 ns	0.34 ns

Figure 5. Results of the SQRT CSLA with the modified full adder design

The comparison graph shown in Figure 7 shows the difference in the area required. From the graphical analysis, it is evident that the area requirement of regular SQRT CSLA is higher when correlated with our modified SQRT CSLA. The RTL schematic of the proposed design is depicted in the Figure 8. Individual ripple carry adder's RTL schematic is shown in Figure 9. The delay results are shown in the Table I. It is clear that there is an impressive reduction in delay for the proposed design when correlated with the regular SQRT CSLA. The graphical analysis of delay is shown in the Figure 10.

IV. CONCLUSION

As the area and delay reduction are the critical issues of normal SQRT CSLA. From the proposed design results, it is concluded that this can be reduced by the proposed design which consists of modified full adder replaced the normal full adder in the ripple carry adder block. The proposed design reduces the LUT count by 4.7% and the delay is reduced by 5.3%. In future work LUT count can be reduced by modifying the binary to excess-1 code converter in the CSLA structure.

REFERENCES

J. Kaur, and L. Sood, "Comparison Between Various Types of Adder Topologies," International Journal of Computer Science Technology, vol. 6, no. 1, pp. 62–66, March 2015.

O. J. Bedrij, "Carry-select adder," IRE Trans. Electron Comput., vol. EC-11, pp. 340–346, June 1962.

S. Manju, V. Sornagopal, "An efficient SQRT architecture of carry select adder design by common Boolean logic," Proc. VLSI ICEVENT, pp. 1–5, 2013.

P. Nautiyal, P. Madduri, and S. Negi, "Implementation of an ALU using modified carry select adder for low power and area-efficient applications," Int. Conf. on Computer and Computational Sciences, Noida, India, pp. 22–25, 2015.

B. Ramkumar, and H. M. Kittur, "Low-Power and Area-Efficient Carry Select Adder". IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 20, no.2, pp. 371–375, Jan. 2011.

R. Priya, and J. S. Kumar, "Implementation and comparison of effective area efficient architectures for CSLA," Proc. IEEE Int. Conf. Emerging Trends Comput. Commun. Nanotechnol., pp. 287–292, Mar. 2013.

G. C. Manjunatha, and R. Singh, "Low Power VLSI Design for Power and Area Effective Utilisation of Carry Select Adder," Int. Conf. on Current Trends in Computer, Electrical, Electronics and Communication, Mysore, India, pp. 606–610, 2017.

N. Patil, A. Joshi, N. Eskandari, and T. Nikoubin, "RCA with conditional BEC in CSLA structure for area-power efficiency," 6th Int. Conf. on Computing, Comm. and Networking Technologies, Denton, USA, pp. 1–4, 2015.

L. Mugilvannan, and S. Ramasamy, "Low-Power and Area-Efficient Carry Select Adder Using Modified BEC-1 Converter", IEEE-31661. 4th ICCCNT 2013, Tiruchengode, India, pp. 1–5, 2013.

S. Nagaraj, G. M. Reddy, and S. A. Mastani, "Analysis of different Adders using CMOS, CPL and DPL logic," 14th IEEE India Council Int. Conf. pp. 1–6, 2017.

T. -. Chang and M. -. Hsiao, "Carry-select adder using single ripple-carry adder," in Electronics Letters, vol. 34, no. 22, pp. 2101–2103, Oct. 1998.

A. Anand Kumar, *Switching Theory and Logic Design*, 2nd ed. Delhi, PHI Learning Private limited, 2014

N. A. Kamsani, V. Thangasamy, Shaiful, M. F. Bukhori, Z. Yusoff, M. N. Hamidon, "A low power multiplexer based pass transistor logic full adder," IEEE Regional Symp. on Micro and Nano electronics (RSM), Kuala Terengganu, Malaysia, pp. 1–4, 2015.

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